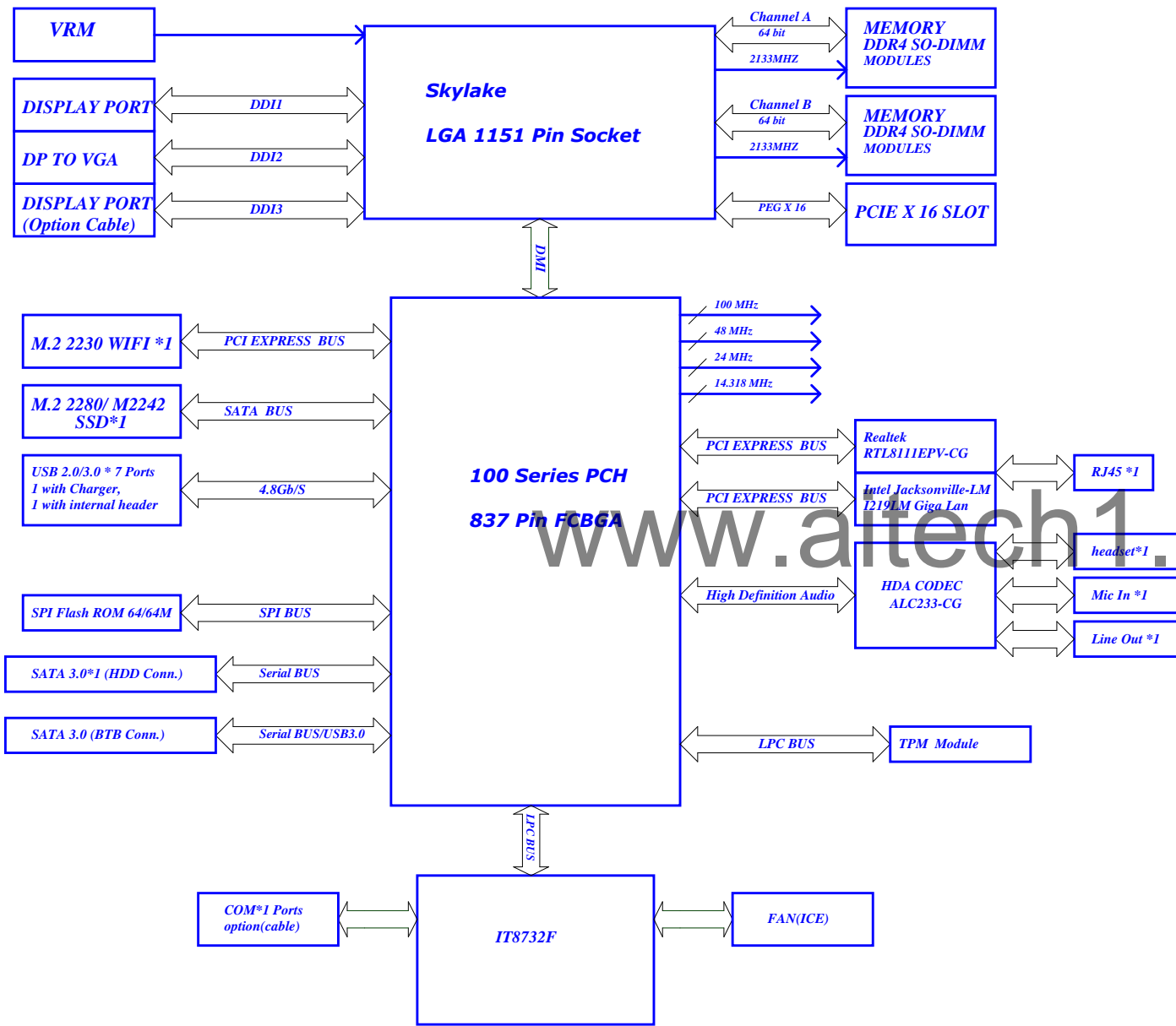


MC110



Project  
Document No :  
X01 :

PAGE	TITLE
01	Block Diagram
02	Power Sequence
03	Power Delivery Map
04	CPU-1: MSIC
05	CPU-2: FDI/PCIE/DMI
06	CPU-3: DDR4 CHA
07	CPU-4: DDR4 CHB
08	CPU-5: Power
09	CPU-6: GND
10	DDR4 CHA SO-DIMM1
11	Blank
12	DDR4 CHB SO-DIMM3
13	Blank
14	PCH-1: DMI/ USB/ LPC/ PCIE
15	PCH-2: PCIE/ SATA/ FAN
16	PCH-3: HDA/ RTC/ SMB/ SPI
17	PCH-4: Display
18	PCH-5: Clock
19	PCH-6: Power 1
20	Blank
21	PCH-8: GND
22	CMOS Clear / Battery/ Buzzer
23	DSW
24	SPI ROM/ XDP_OP
25	BLANK
26	Display Port B
27	Display to VGA
28	Display Port D(Optional)
29	Audio Codec - ALC233-CG
30	Audio Jack Line I-O/ Mic in
31	SIO IT8732F
32	Rear USB3.0/2.0 x3
33	FAN CTRL
34	TPM - TCG 2.0
35	LAN - Jacksonville_i219LM
36	RJ45 & Realtek RTL8111EP #
37	USB2.0/COM PORT(Optional)
38	Front USB3 x 2
39	Front USB3 Charger x1
40	M.2 2230-E WIFI/ BT
41	M.2 2280-M SSD
42	PCIE X16
43	SATA HDD/Extension Box
44	PWRGD
45	Button/ LED
46	SM BUS/Thermal Sensing/APS
47	Debug Port
48	Mounting Hole/ PCB/ Metal
49	Blank
50	+20V_S5_ADP
51	+5V_S5/+3V3_S5
52	+3V3_DSW/+5V/+3V3
53	+12V
54	VCORE CONTROLLER
55	VCCIA Output
56	VCCGT Output
57	+1V2_DDR / +0V6_VTT
58	+2V5_VPP
59	+1V0_PCH_PRIME
60	+VCCIO
61	+VCCSA
62	Blank

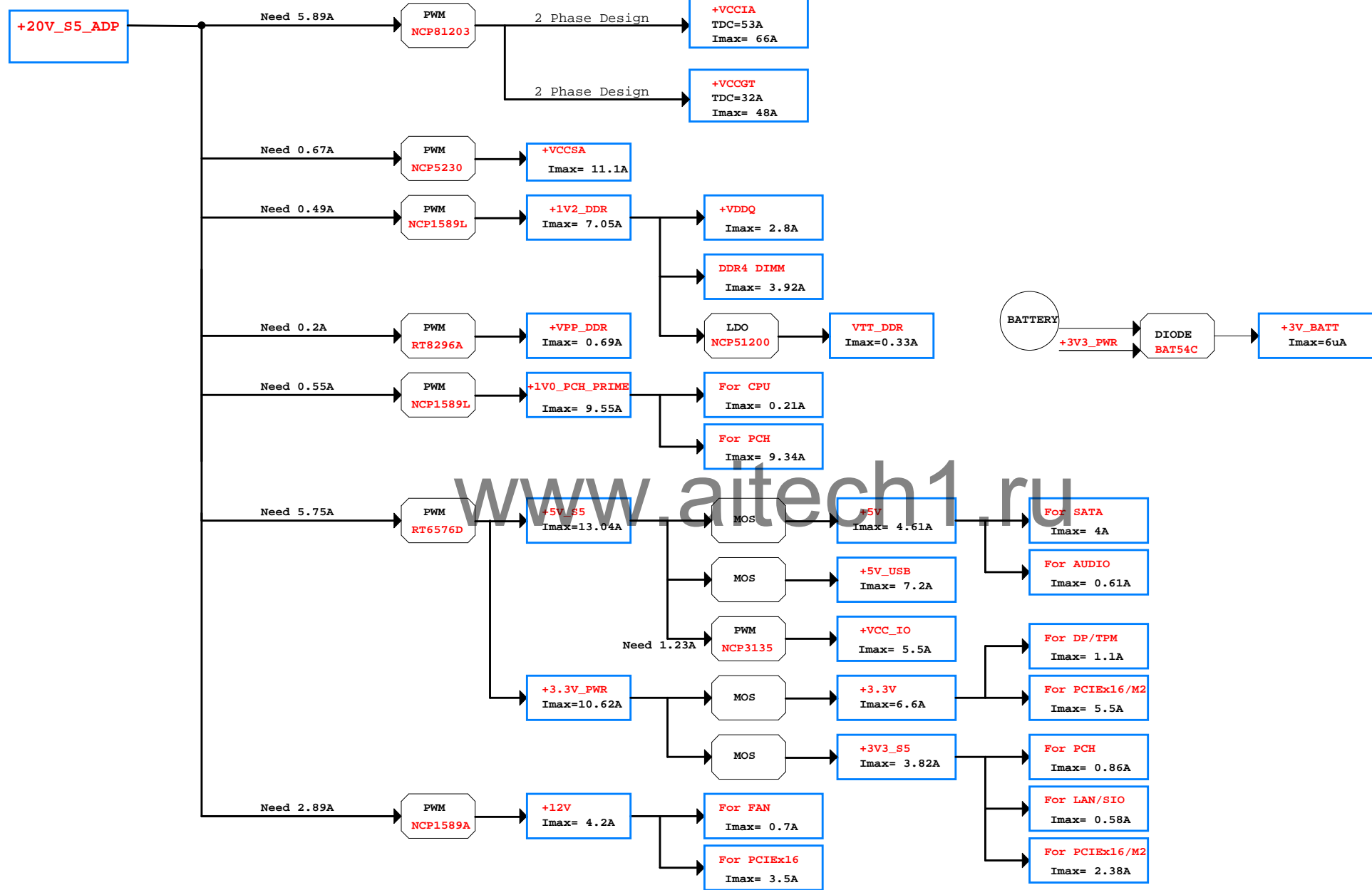


DSW/PRIM VRs and DSW\_PWROK/RSMRST# logic not shown

The diagram illustrates the SLP\_SUS# signal path. It starts with 'Other S5 VRs' providing EN\_PSG signals to three VCCPRIM regulators (1.0A, 1.0V, and 3.3V) and a DSW (3.3V) regulator. Each regulator has a 'PWRGOOD' output. These PWRGOOD signals, along with 'Other PwrGood signals feeding into ALL\_SYS\_PWRGD', are connected to Node 4 via inverters. Node 4 is connected to ALL\_SYS\_PWRGD. The 3.3V VCCPRIM PWRGOOD signal is also connected to Node 5 via an inverter. Node 5 is connected to the 'To Board Logic/EC' and the SWAY10M pin. The SWAY10M pin is connected to the RSMRST# pin of the SPT-H component. The RSMRST# pin is also connected to the SLP\_SUS# pin of the SPT-H component. The SLP\_SUS# pin is also connected to the SLP\_SUS# pin of the SPT-H component. The SLP\_SUS# signal is also connected to the SLP\_SUS# pin of the SPT-H component.

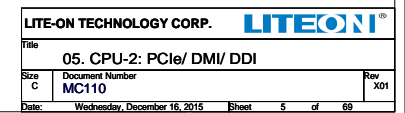
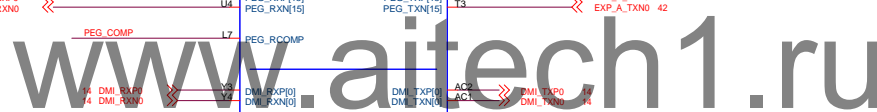
Rails	S0/M0	S3/M3	S4/M3	S5/M3	Sx/M-Off	Deep S3	Deep S4/S5	G3
RTC Well	ON	ON	ON	ON	ON	ON	ON	ON
PS_SVSB	ON	ON	ON	ON	ON	ON	ON	ON
3.3V_DSW	ON	ON	3.3V_DSW	ON	ON	ON	ON	No Pow
VBATA (VDC) <sup>12</sup>	ON	ON	ON	ON	ON	ON	ON	No Pow
V5.0A	ON	ON	ON	ON	ON	OFF	OFF	No Pow
V3.3A	ON	ON	ON	ON	ON	OFF	OFF	No Pow
V1.8A <sup>13</sup>	ON	ON	ON	ON	ON	OFF	OFF	No Pow
V1.0A	ON	ON	ON	ON	ON	OFF	OFF	No Pow
VCCOPC_1p8	ON	ON <sup>15</sup>	ON <sup>15</sup>	ON <sup>15</sup>	ON <sup>15</sup>	OFF	OFF	No Pow
V3.3M <sup>3</sup>	ON	ON <sup>11</sup>	ON <sup>11</sup>	ON <sup>11</sup>	OFF	OFF	OFF	No Pow
V1.8M <sup>3</sup>	ON	ON <sup>11</sup>	ON <sup>11</sup>	ON <sup>11</sup>	OFF	OFF	OFF	No Pow
VDDQ	ON	ON	OFF	OFF	OFF	ON	OFF	No Pow
V1.8U/V2.5U	ON	ON	OFF	OFF	OFF	ON	OFF	No Pow
VCCST	ON	ON	OFF <sup>5</sup>	OFF <sup>5</sup>	OFF <sup>5</sup>	OFF	OFF	No Pow
VCCPLL	ON	ON <sup>7</sup>	OFF <sup>5</sup>	OFF <sup>5</sup>	OFF <sup>5</sup>	OFF <sup>5</sup>	OFF	No Pow
VCCPLL_OC	ON	ON <sup>8</sup>	OFF	OFF	OFF	OFF <sup>8</sup>	OFF	No Pow
V3.3S	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Pow
V5.0S	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Pow
VCC	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Pow
VCCGT/VCCGTx	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Pow
VCCIO	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Pow
VCCSA	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Pow
VCCOPC	ON/OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Pow
VCCOEPIO	ON/OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Pow
P12V, PSV, P3V3	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Pow

# POWER CONN



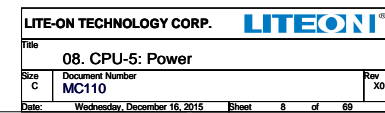
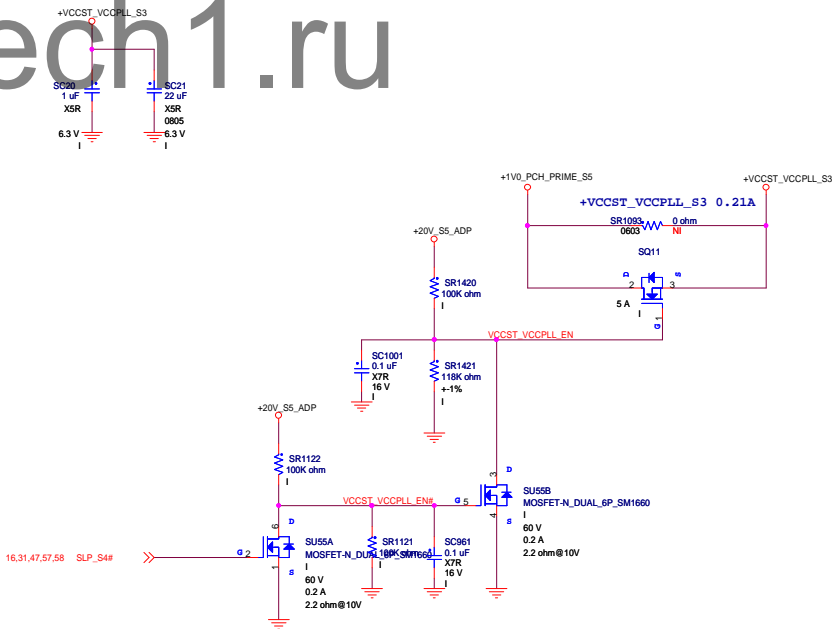


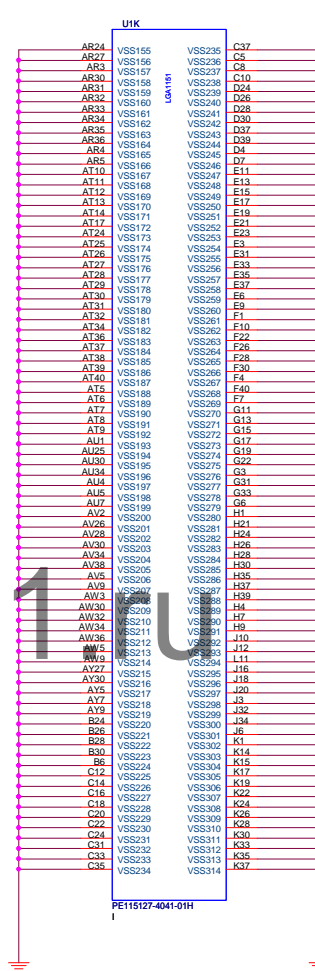
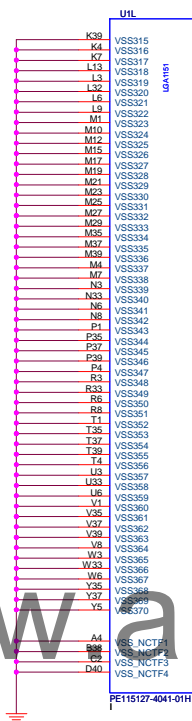
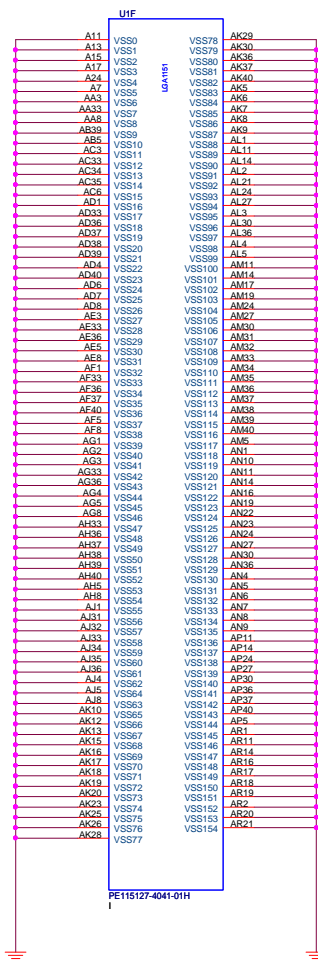


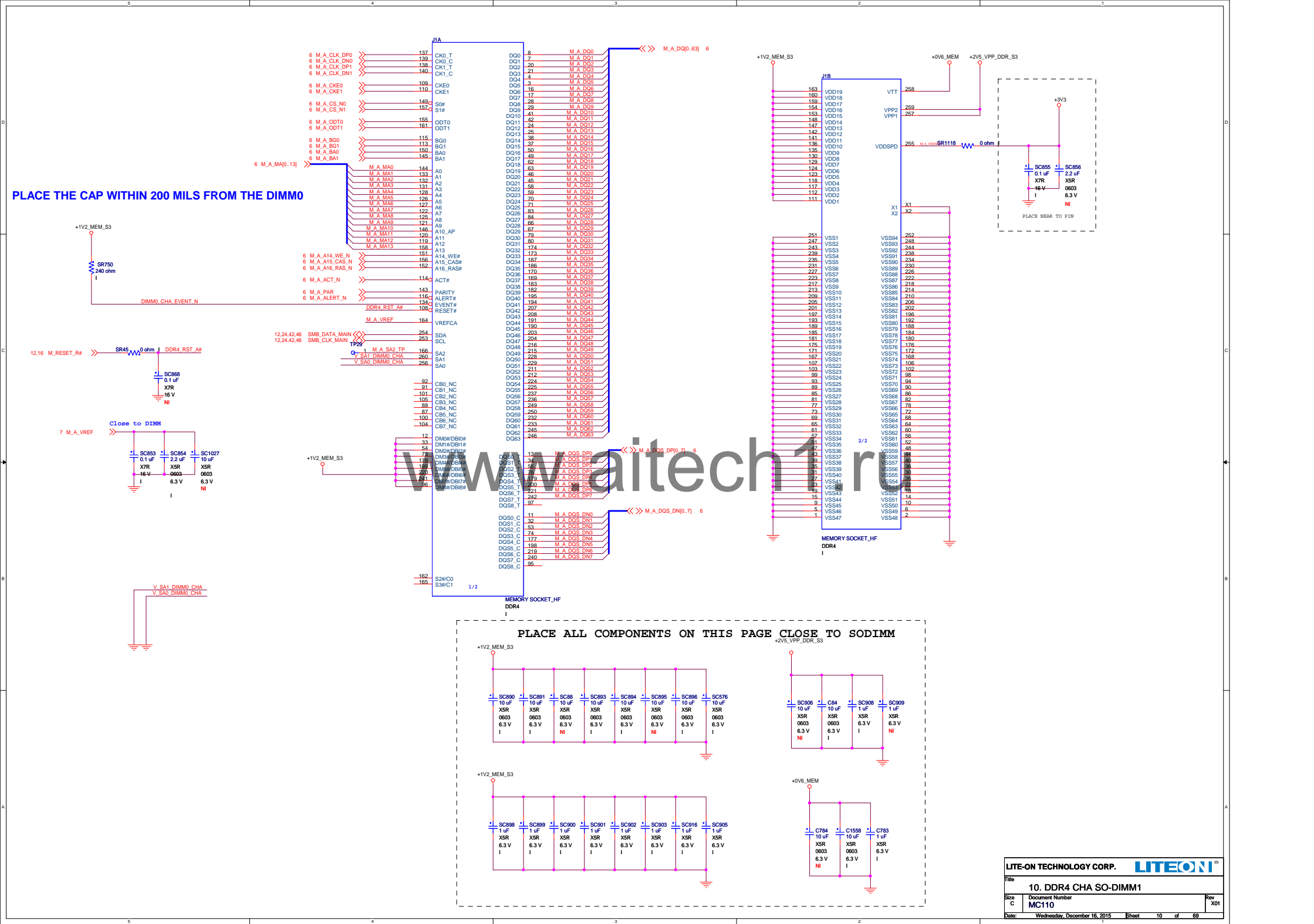




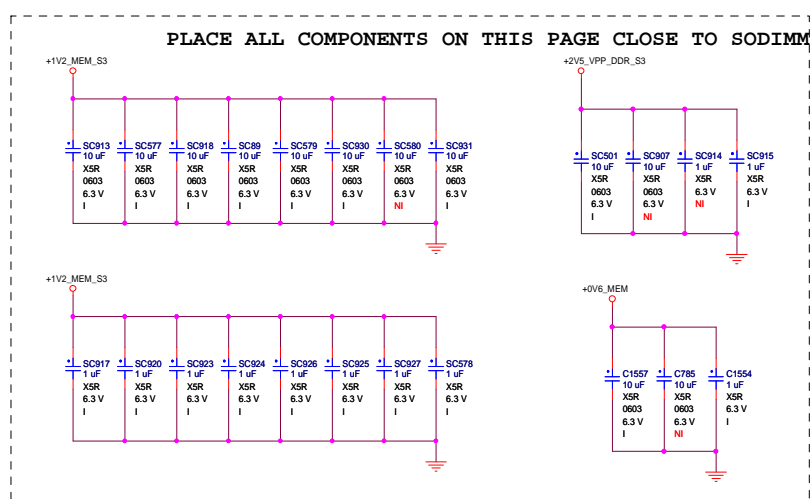






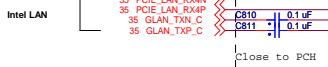


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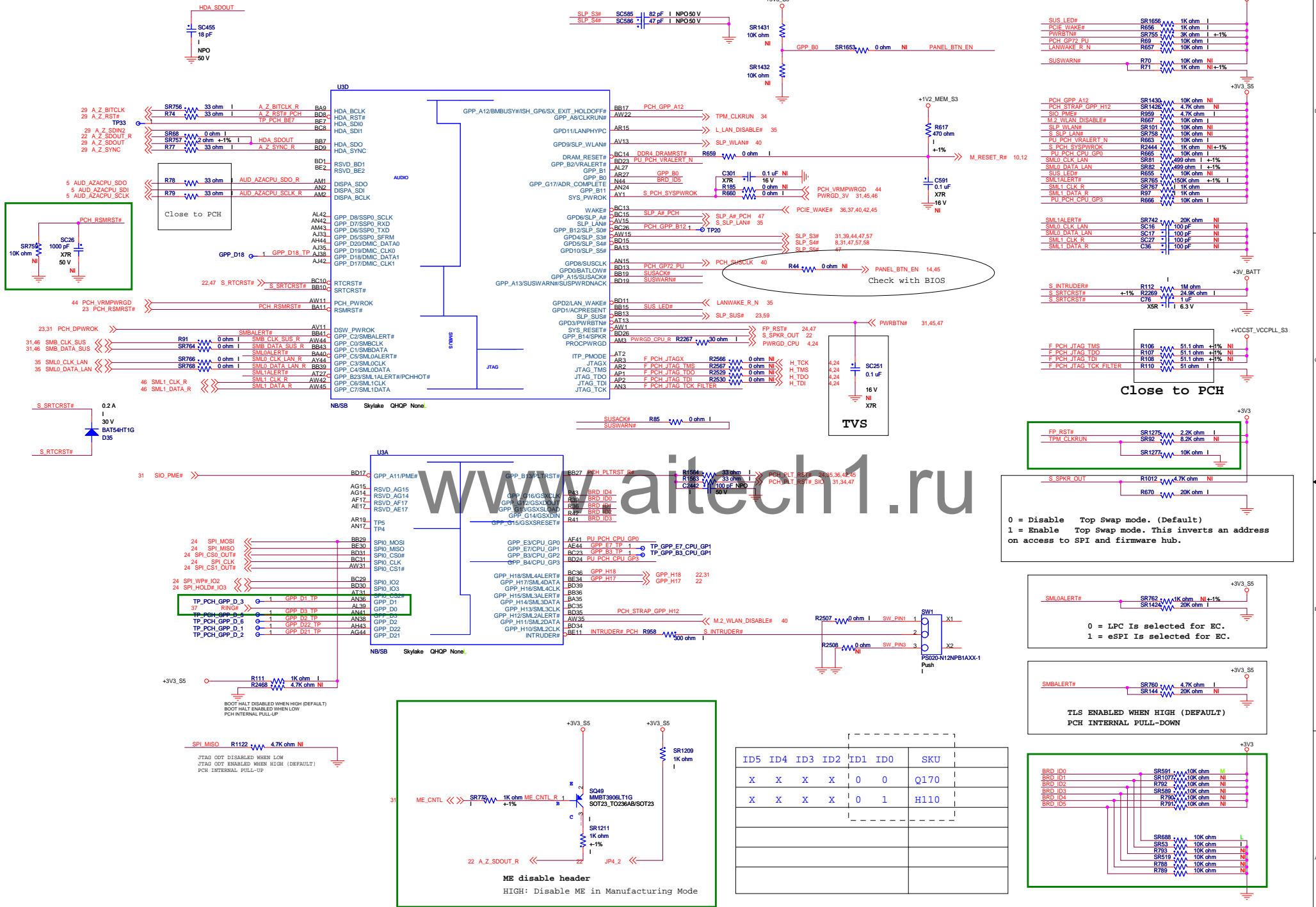
Features	H110	H170	HM170	QM170	Z170	B150	Q150	Q170
Intel® Rapid Storage Technology	AHCI Mode	Full Features	Full Features	Full Features	Full Features	AHCI Mode	AHCI Mode	Full Features
Total USB 3.0 Ports	4	8	8	8	10	6	8	10
Total USB 2.0 Ports	10 <sup>1</sup>	14 <sup>3</sup>	12 <sup>2</sup>	12 <sup>2</sup>	14 <sup>3</sup>	12 <sup>2</sup>	14 <sup>3</sup>	14 <sup>3</sup>
Total SATA 3.0 Ports (Max 6 Gb/s)	4	6	4	4	6	6	6	6
Total PCI Express® Lanes (Gen)	6 (2.0)	16 (3.0)	16 (3.0)	16 (3.0)	20 (3.0)	8 (3.0)	10 (3.0)	20 (3.0)
Total Intel® RST capable PCIe and SATA Express <sup>4</sup> Storage Devices	0	2 <sup>6</sup>	2 <sup>6</sup>	2 <sup>6</sup>	3 <sup>7</sup>	0	0	3 <sup>7</sup>
SKL Processor dfgk bifurcation support	No	No	Yes <sup>4</sup>	Yes <sup>4</sup>	Yes <sup>4</sup>	No	No	Yes <sup>5</sup>

**Notes:**

1. USB 2.0 port numbers: 1-10
2. USB 2.0 port numbers: 1-12
3. USB 2.0 port numbers: 1-14
4. SATA Express Capable Ports (x2)
5. PCIe configuration 1x16, or 2x8 or 2x4 or 1x8 are supported
6. Intel® RST PCIe supports RAID configuration 0/1
7. Intel® RST PCIe supports RAID configuration 0/1/5.

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
H170	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
HM170	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	PCIe	PCIe / LAN	PCIe/ LAN	PCIe	PCIe	PCIe
QM170	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	PCIe	PCIe / LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Z170	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
B150	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
Q150	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
Q170	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe/ LAN	PCIe / LAN	PCIe	PCIe	PCIe



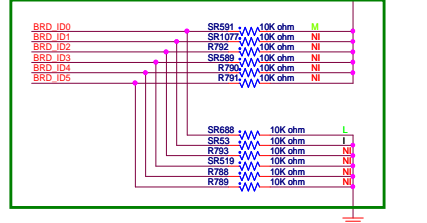


ID5	ID4	ID3	ID2	ID1	ID0	SKU
X	X	X	X	0	0	Q170
X	X	X	X	0	1	H110

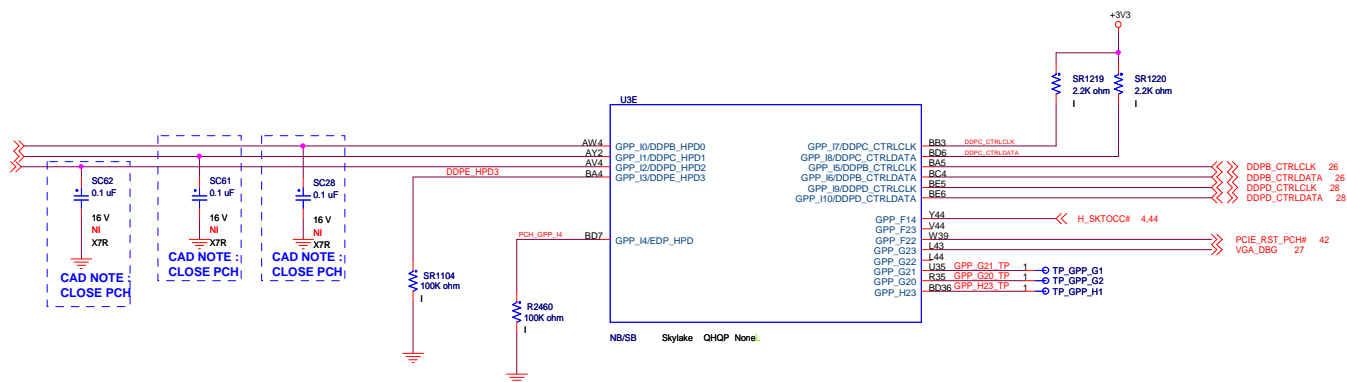
0 = Disable Top Swap mode. (Default)  
1 = Enable Top Swap mode. This inverts an address on access to SPI and firmware hub.

0 = LFC Is selected for EC.  
1 = eSPI Is selected for EC.

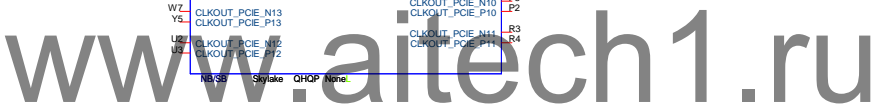
TLS ENABLED WHEN HIGH (DEFAULT)  
PCH INTERNAL PULL-DOWN



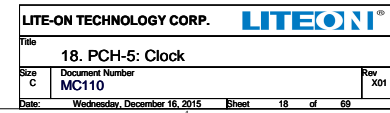
26 DDPB\_HPD\_PD  
27 DDPB\_HPD\_PD  
28 DDPB\_HPD\_PD



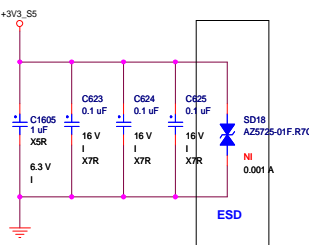
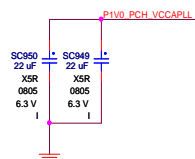
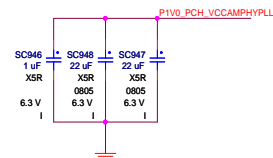
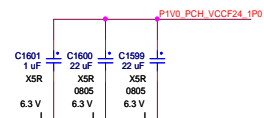
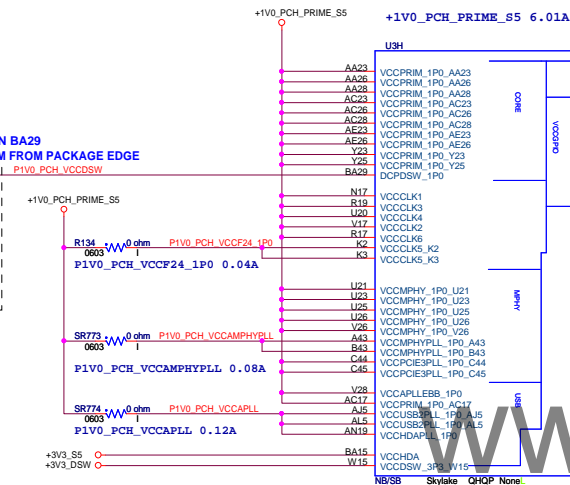
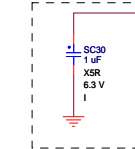
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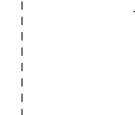
Resistor	Value	Location	Pin
SR1111	22 ohm	CK_LPC1_24M_DEBUG	47
R1109	22 ohm	CK_LPC1_24M_TPM	34
SR1108	22 ohm	CK_LPC0_24M_PCICLK	31



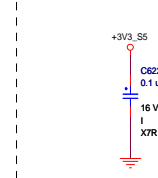
BOARD CAP FOR PIN BA29  
PLACE WITHIN 3-5 MM FROM PACKAGE EDGE



BOARD CAP FOR PIN AD13  
PLACE WITHIN 3-5 MM FROM PACKAGE EDGE



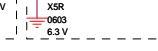
BOARD CAP FOR PIN BC40 BD40  
PLACE WITHIN 3-5 MM FROM PACKAGE EDGE



EDGE CAP FOR VCCMPHY\_1P0  
PIN U26, U25, U23, U21, V26  
PLACE WITHIN 1-3 MM FROM PACKAGE EDGE



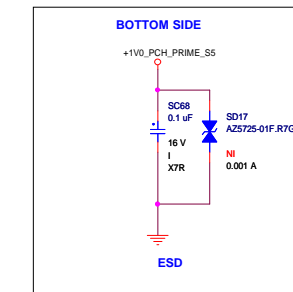
BOARD CAP FOR VCCMPHY\_1P0  
PIN U26, U25, U23, U21, V26  
PLACE WITHIN 3-5 MM FROM PACKAGE EDGE



BOARD CAP FOR PIN BA20  
PLACE WITHIN 3-5 MM FROM PACKAGE EDGE

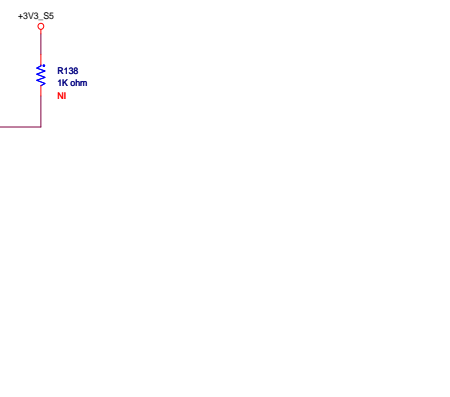
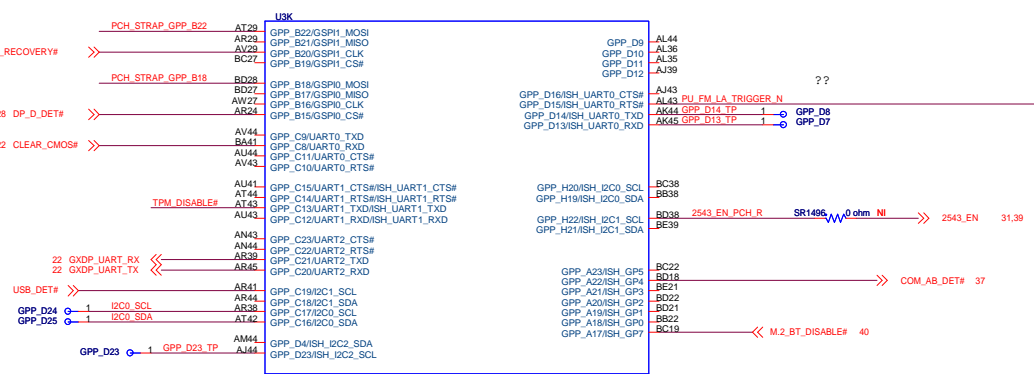
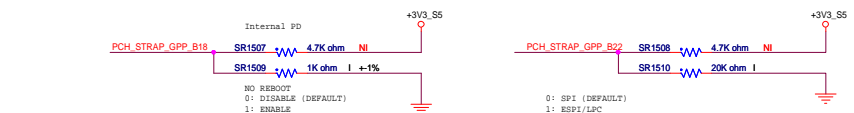
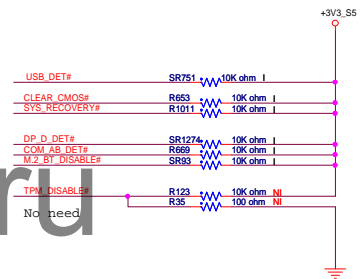
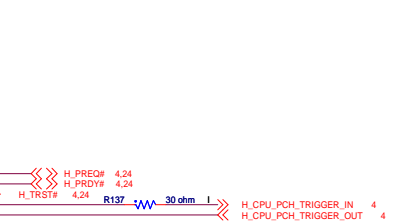
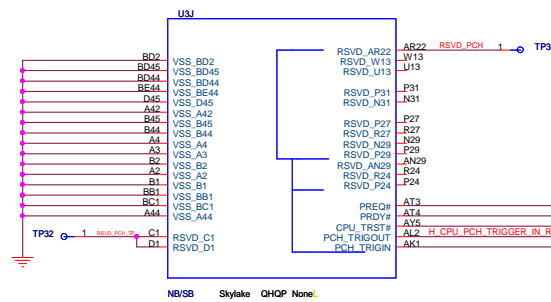


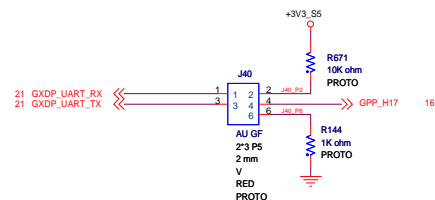
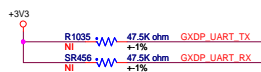
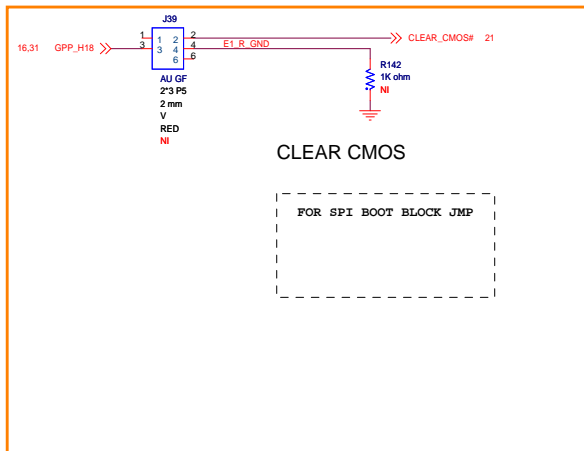
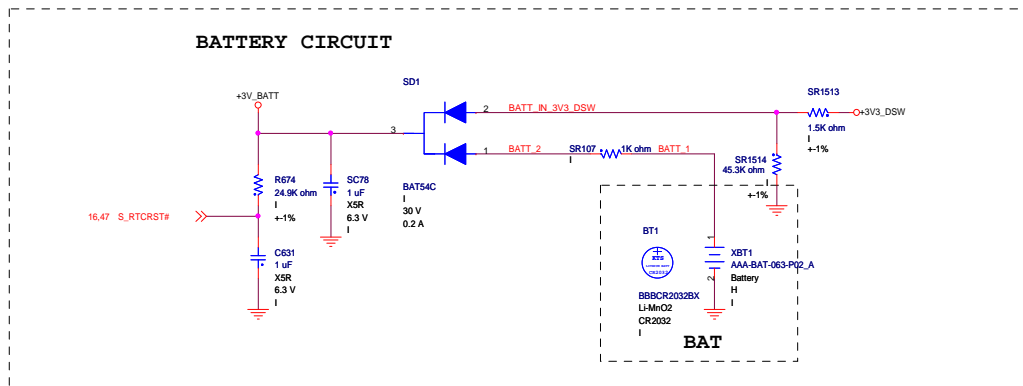
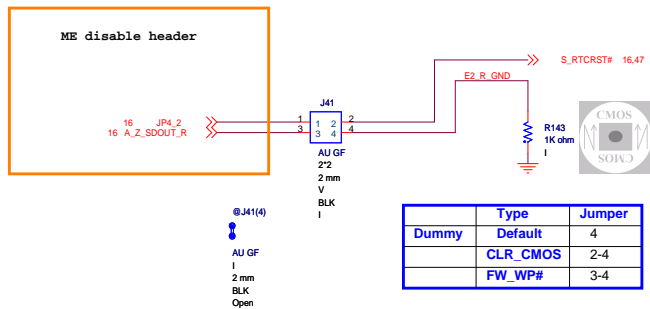
EDGE CAP FOR PIN BA22  
PLACE WITHIN 3-5 MM FROM PACKAGE EDGE



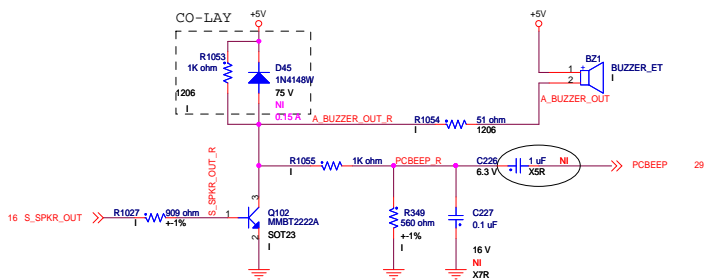
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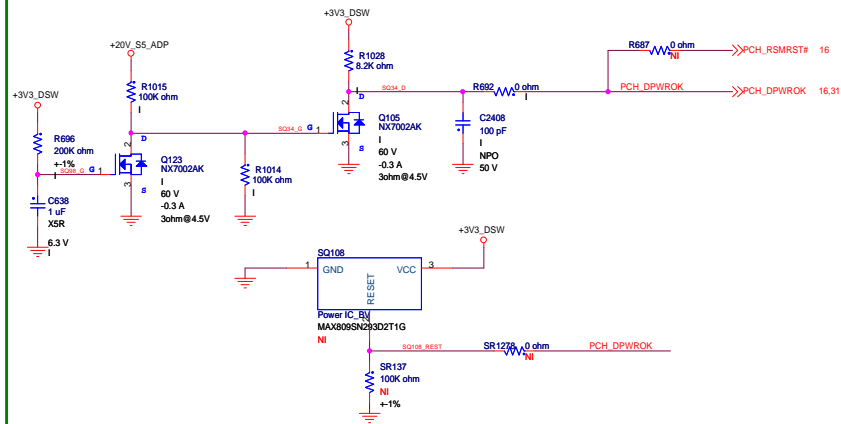




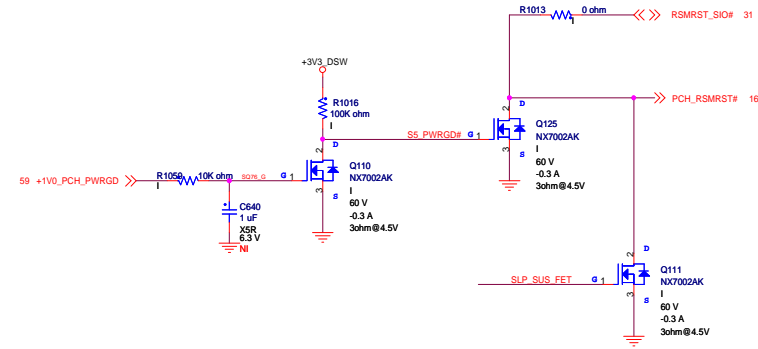
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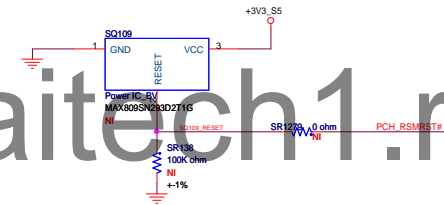
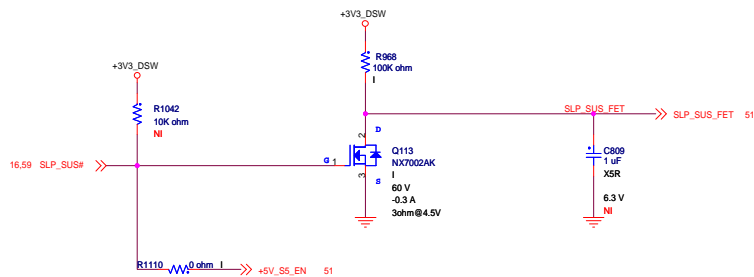
## PCH\_DPWR0K



RSMRST\_SIO# De-active delay form  
+3V3B= +3V3\_S5 -->75mS

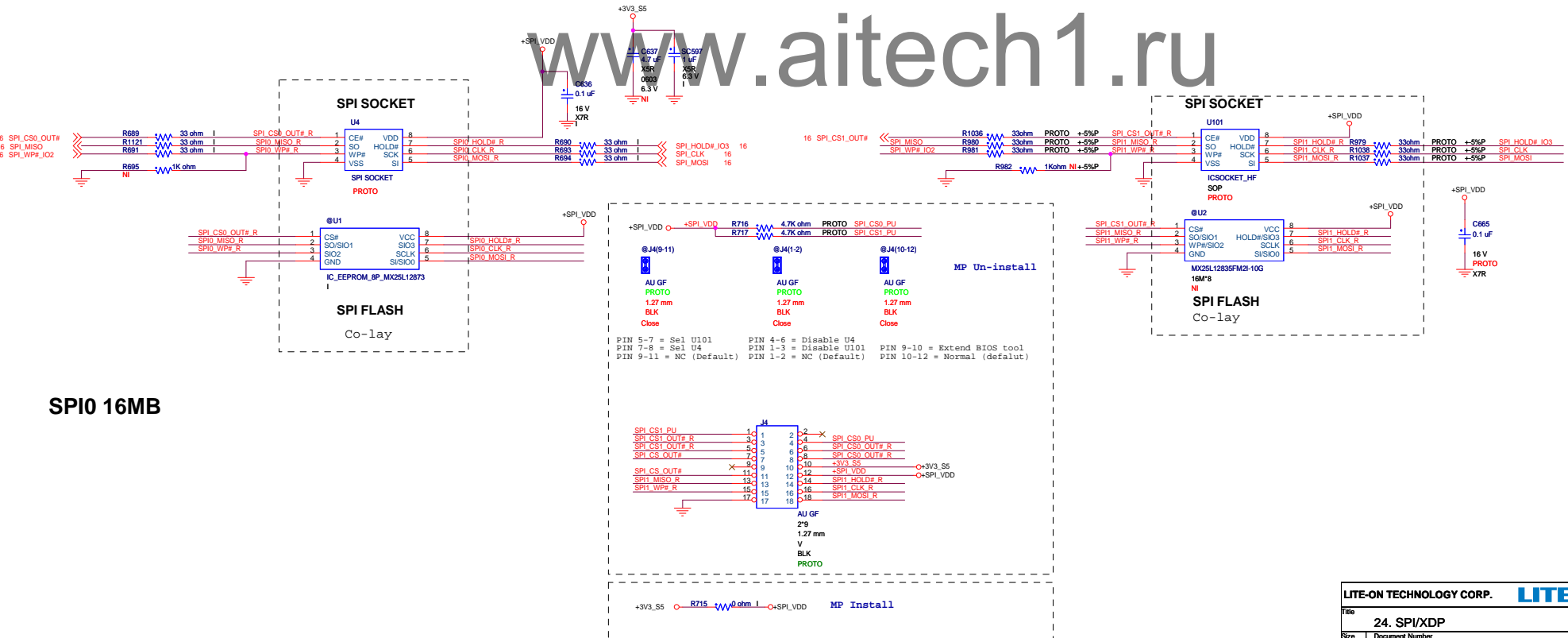
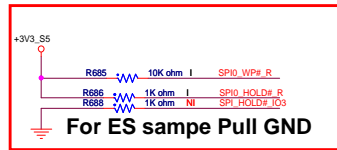
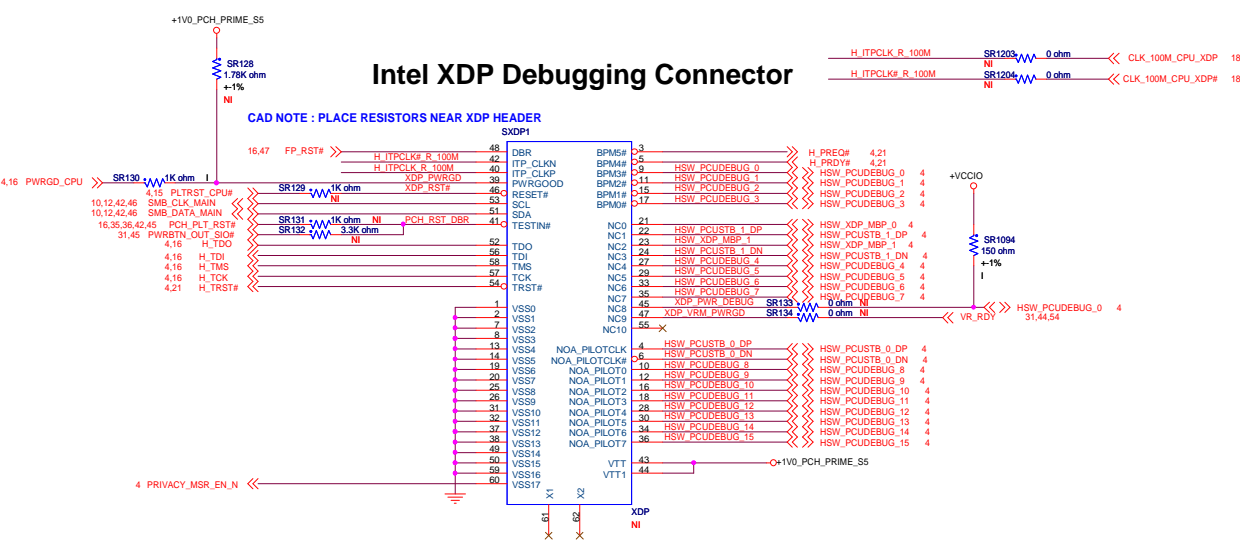


## DSW CONTROL SIGNAL




# Intel XDP Debugging Connector

CAD NOTE : PLACE RESISTORS NEAR XDP HEADER

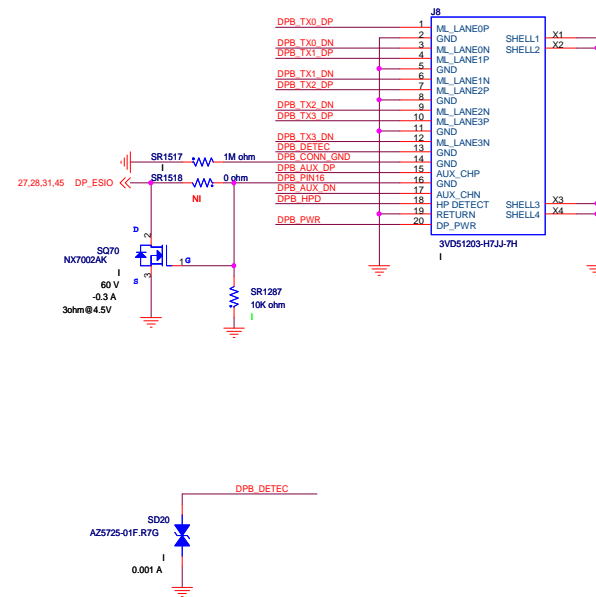


SPI0 16MB

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LITE-ON TECHNOLOGY CORP.			
Title			
25. Blank			
Size	Document Number		Rev
C	MC110		X01
Date:	Wednesday, December 16, 2015	Sheet	25 of 69

5	DDSP_8_DP_0, 0, 1	>>>	C670	0.1_UF	16_V	X7R	DPB	TX0	DP
6	DDSP_8_DP_0, 0, 0	>>>	C671*	0.1_UF	16_V	X7R	DPB	TX0	DN
7	DDSP_8_DP_0, 1, 0	>>>	C672*	0.1_UF	16_V	X7R	DPB	TX1	DP
8	DDSP_8_DP_1, 0, 1	>>>	C673*	0.1_UF	16_V	X7R	DPB	TX1	DN
9	DDSP_8_DP_2, 2, 0	>>>	C674*	0.1_UF	16_V	X7R	DPB	TX2	DP
10	DDSP_8_DP_2, 2, 0	>>>	C675*	0.1_UF	16_V	X7R	DPB	TX2	DN
11	DDSP_8_DP_3, 3, 0	>>>	C676	0.1_UF	16_V	X7R	DPB	TX3	DP
12	DDSP_8_DP_3, 3, 0	>>>	C677*	0.1_UF	16_V	X7R	DPB	TX3	DN



**Aux Channel Control**

HPD PASS GATE - Pass gate to prevent back-drive when sink device is on and PCH is powered down

5V

3V3

16V

R2282 1K ohm

R2283 1K ohm

R2284 1M ohm

SR1317 1K ohm

DP I, HDMI NI

DBP DETEC

DBP\_AUX\_DP

DBP\_AUX\_DN

DDPB\_CTRL\_ENH

R1118 100K ohm

C2384 0.1 uF

R2496 2.2K ohm

R2497 2.2K ohm

U100 C8T3257ADS

Input		Function
OE	S	A port = B1 port
L	L	A port = B2 port
L	H	Disconnect
H	X	

DBPB\_CTRLCLK 17

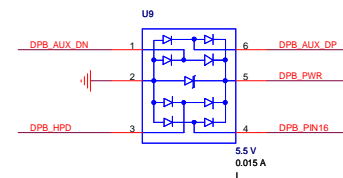
DDPB\_CTRLDATA 17



DDPB\_B\_AUX\_DP\_C SC1006 0.1 uF 16V I XTR

DDPB\_B\_AUX\_DN\_C SC1007 0.1 uF 16V I XTR

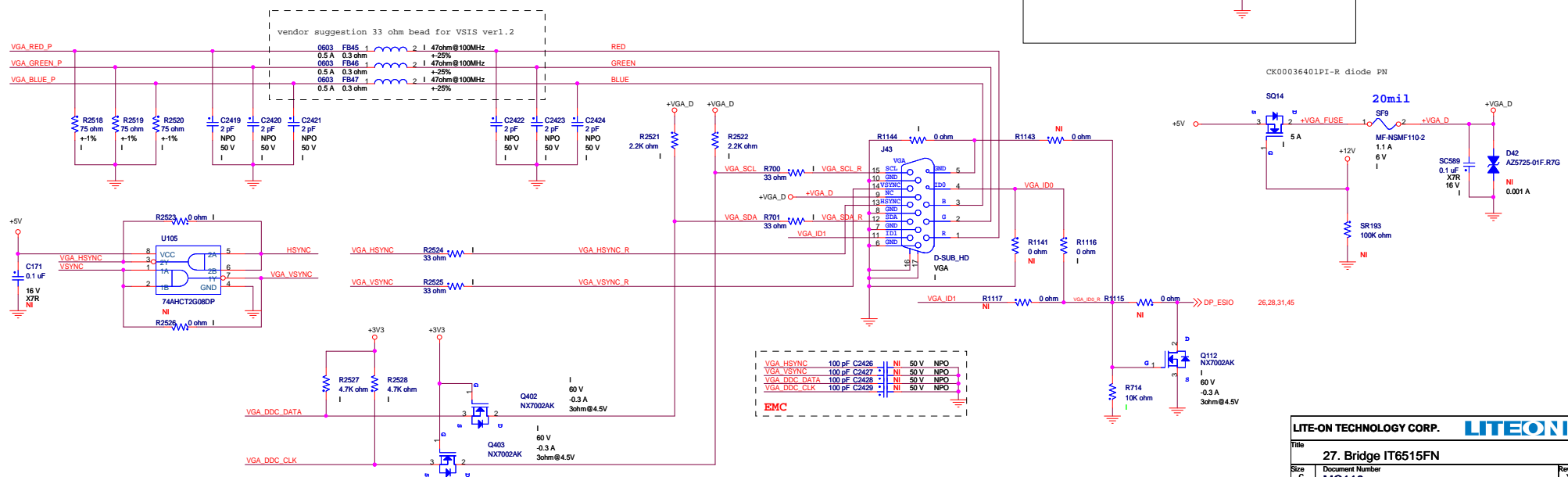
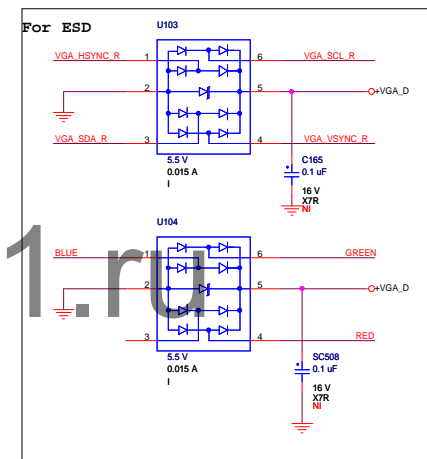
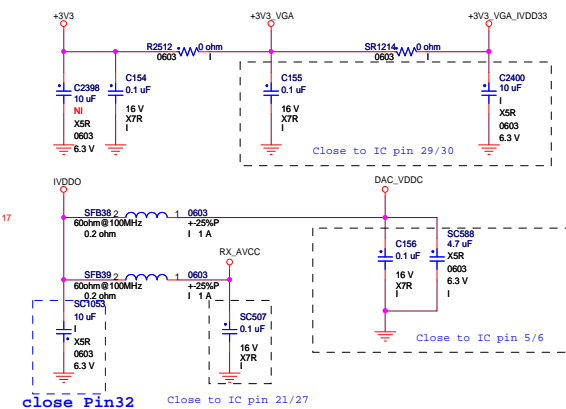
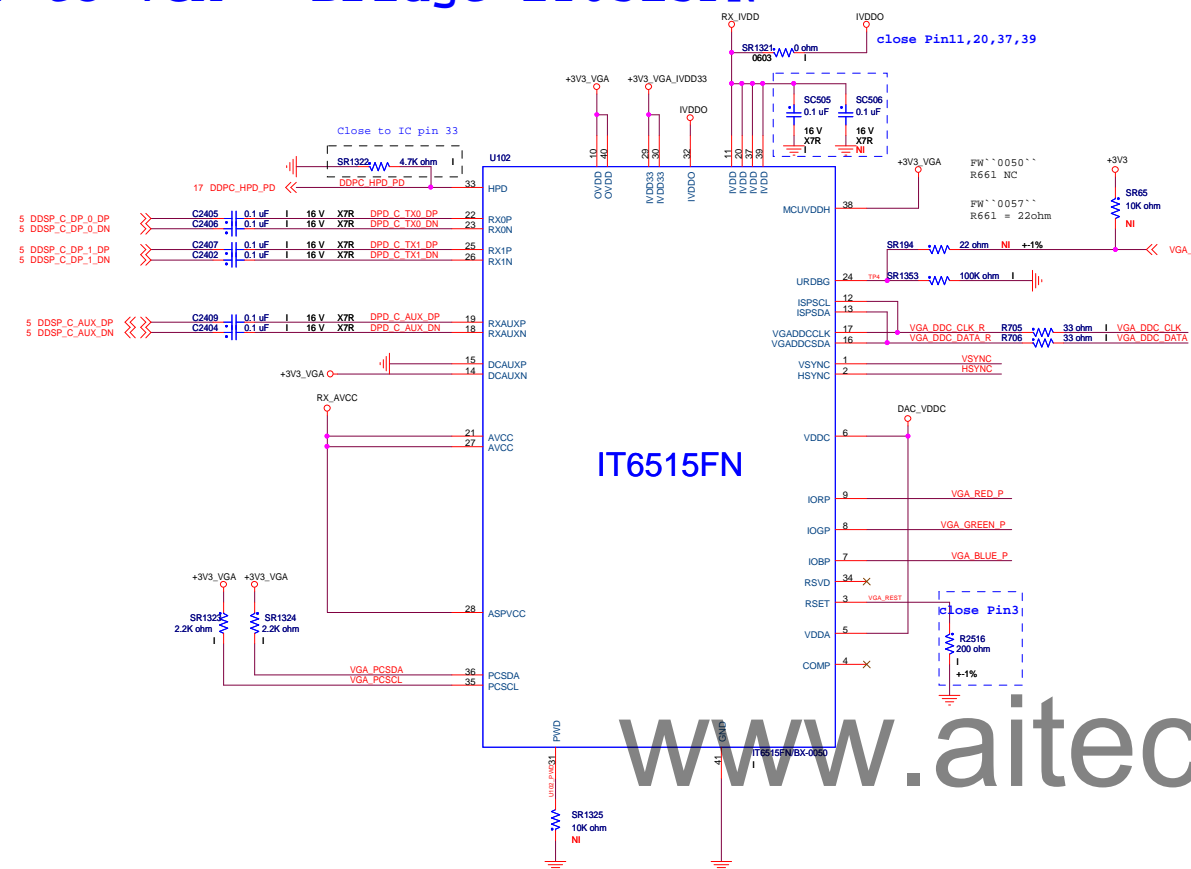
DDPB\_B\_AUX\_DP 5

DDPB\_B\_AUX\_DN 5



 	
Title	
26. Display Port B	
Size	Document Number
C	MC110
	Rev X01
Date:	Wednesday, December 16, 2015
Sheet	26 of 69

## DP to VGA - Bridge IT6515FN



### DISPLAY PORT

HPD PASS GATE -  
Pass gate to prevent  
back-drive when sink  
device is on and  
PCH is powered  
down

17 DPDP\_HPD\_PD <<

5 DDSP\_D\_DP\_0\_DP >> SC49 0.1 uF 16 V X7R DPD\_TX0\_DP  
5 DDSP\_D\_DP\_0\_DN >> SC50 0.1 uF 16 V X7R DPD\_TX0\_DN  
5 DDSP\_D\_DP\_1\_DP >> SC51 0.1 uF 16 V X7R DPD\_TX1\_DP  
5 DDSP\_D\_DP\_1\_DN >> SC52 0.1 uF 16 V X7R DPD\_TX1\_DN  
5 DDSP\_D\_DP\_2\_DP >> SC53 0.1 uF 16 V X7R DPD\_TX2\_DP  
5 DDSP\_D\_DP\_2\_DN >> SC54 0.1 uF 16 V X7R DPD\_TX2\_DN  
5 DDSP\_D\_DP\_3\_DP >> SC55 0.1 uF 16 V X7R DPD\_TX3\_DP  
5 DDSP\_D\_DP\_3\_DN >> SC56 0.1 uF 16 V X7R DPD\_TX3\_DN

DPDP\_HPD

DPDP\_PIN14

3V3

SR1208 1M ohm

SQ54 NX7002AK 60 V -0.3 A 3ohm@4.5V

SR1316 20K ohm

SC56 0.1 uF 16 V X7R

R203 1M ohm

3V3

20MIL

SQ13

5 A

3V3

DPDP\_PWR\_3V3

SF2 MF-NSMF110-2 1.1 A 6 V

SR1213 0603 0 ohm

DPDP\_PWR\_L

DPDP\_PWR

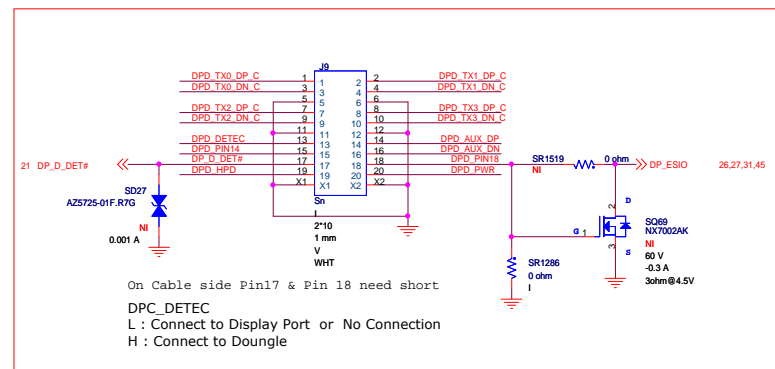
SC111 4.7 uF XSR 0603 6.3 V

SC112 0.1 uF 16 V X7R

SR217 100K ohm

12V

HPD PASS GATE -  
Pass gate to prevent  
back-drive when sink  
device is on and  
PCH is powered  
down



On Cable side Pin17 & Pin 18 need short

DPC DETEC

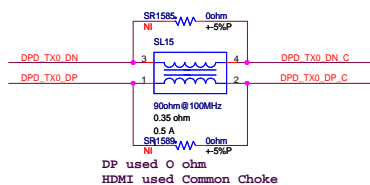
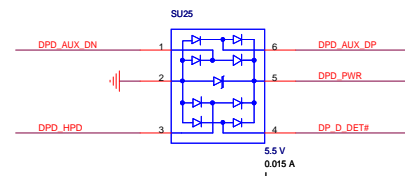
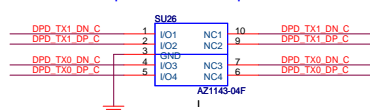
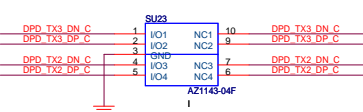
L : Connect to Display Port or No Connection

H : Connect to Dounple

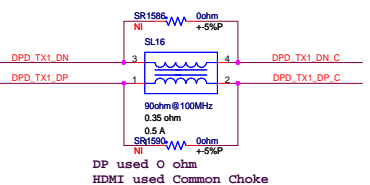
[illegible]

Input		Function
OE	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

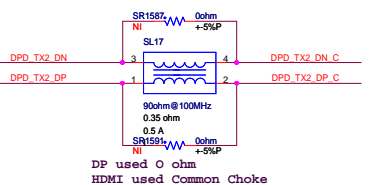
CAD Note : Please place ESD component close to DP connector



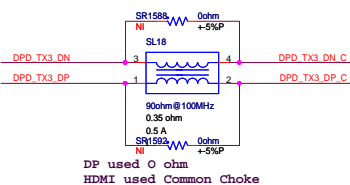
DP used 0 ohm  
HDMI used Common Choke



HDMI used Common Choke



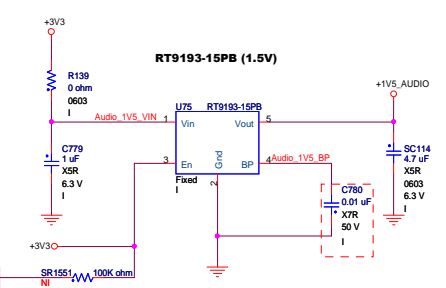
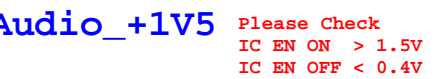
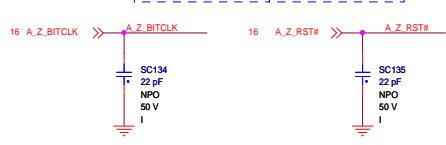
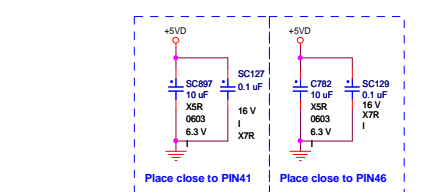
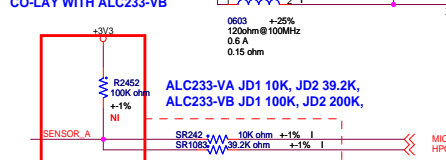
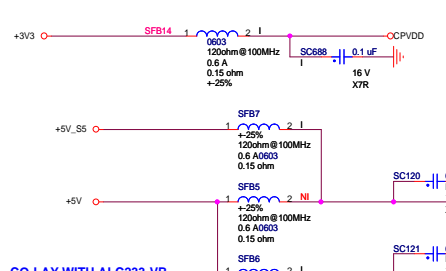
HDMI used Common Choke

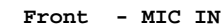


DP used 0 ohm  
HDMI used Common Choke

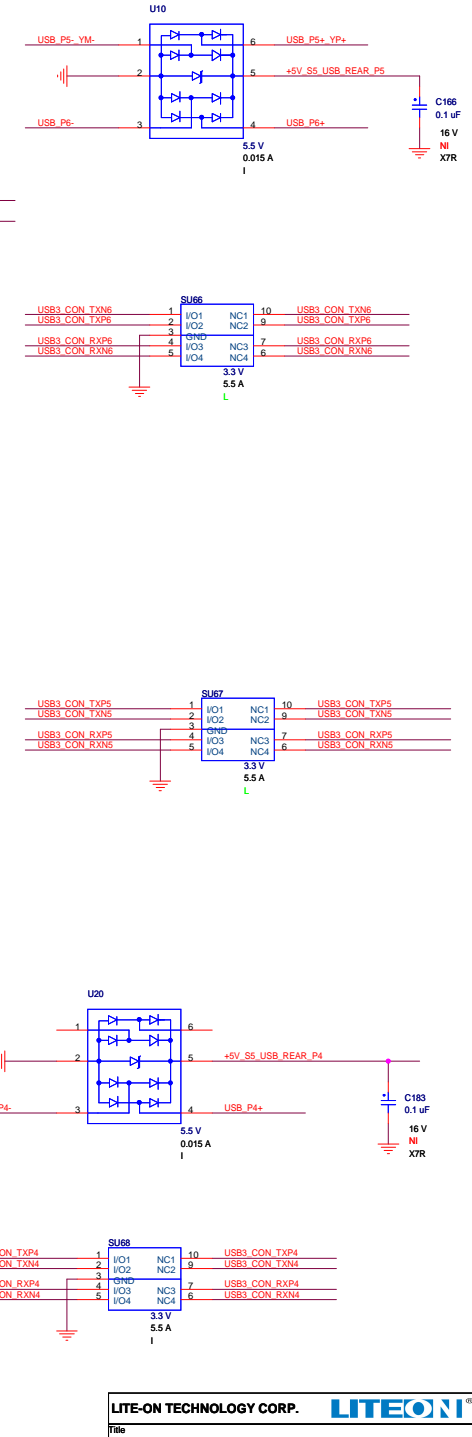
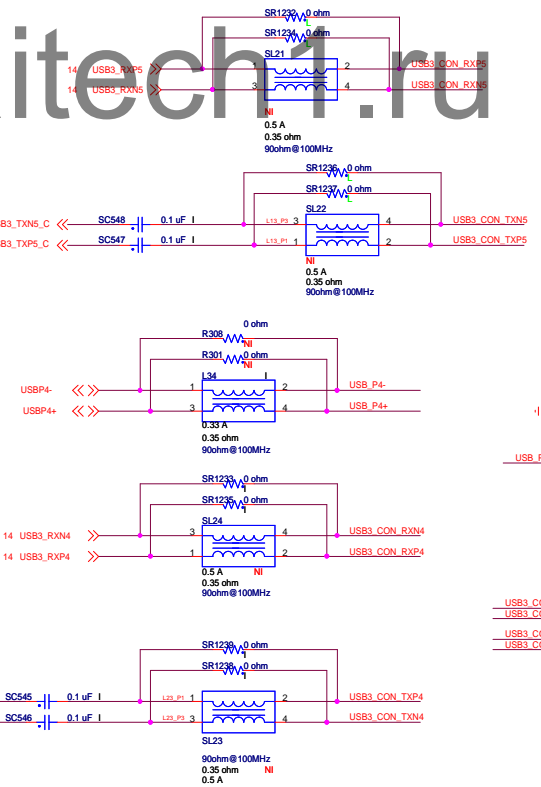
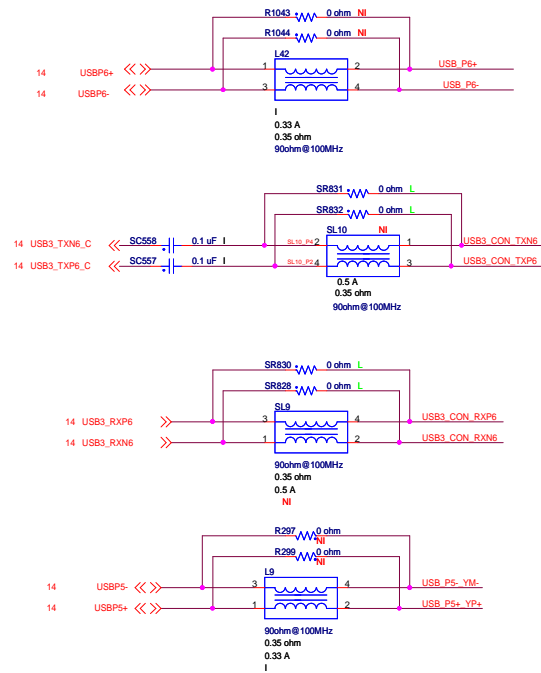
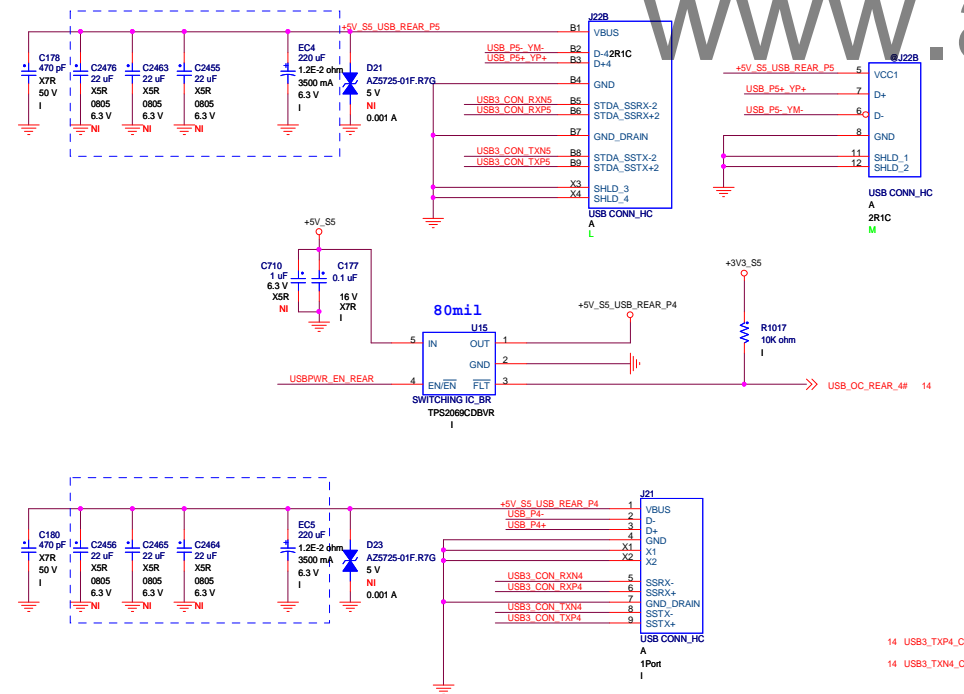
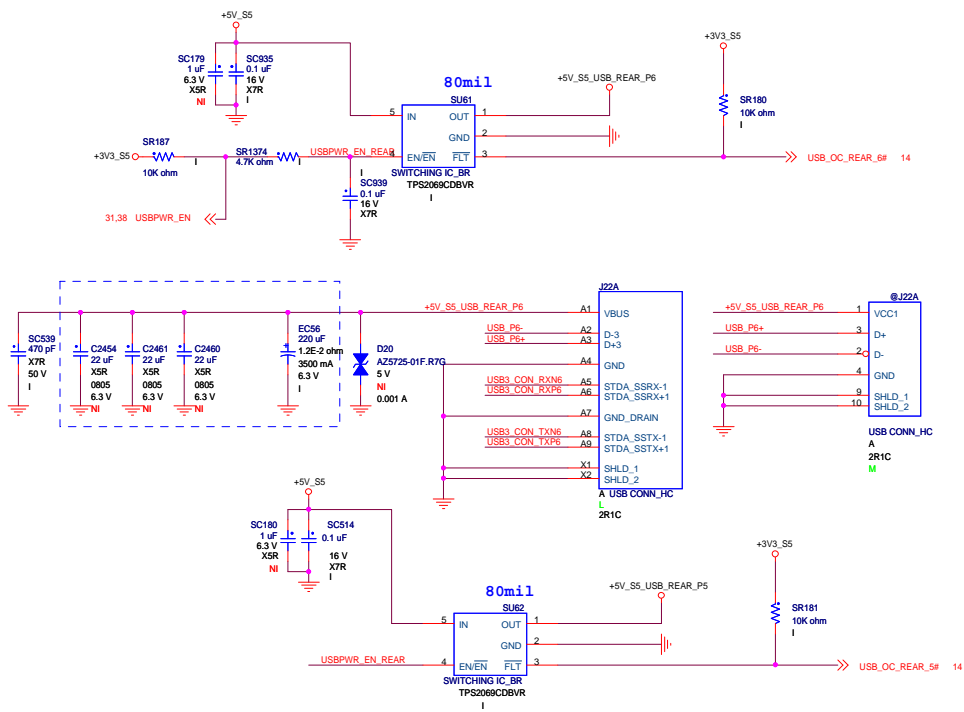
CAD Note : Please place Common Choke component close to J9 pinheader



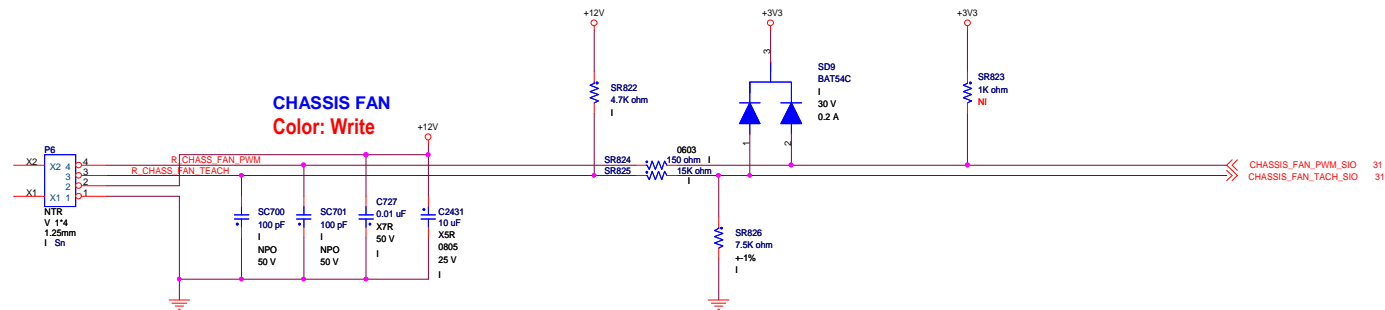








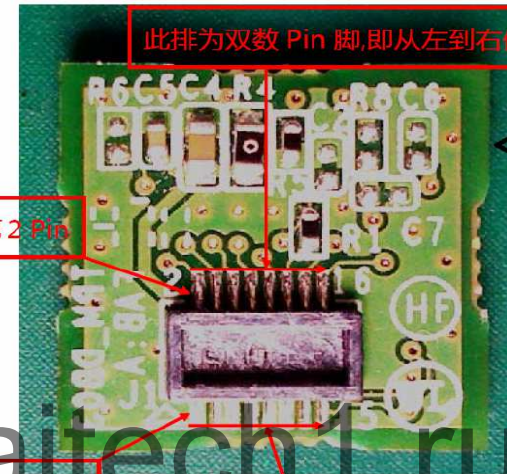
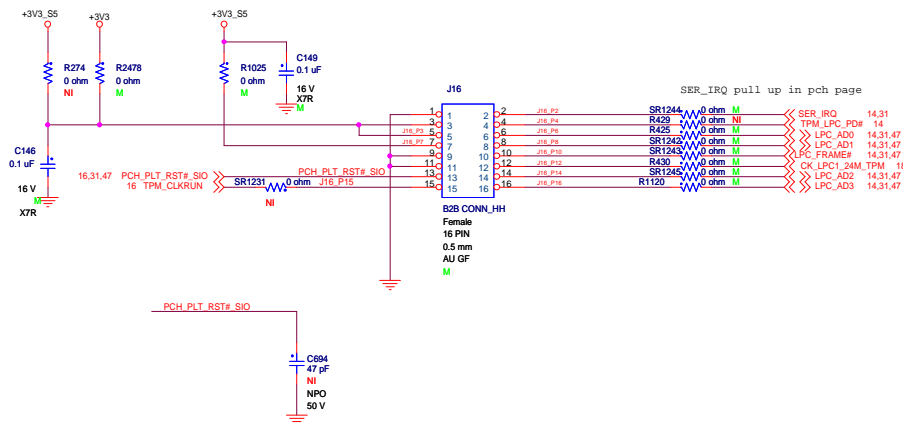
CHASSIS/CPU/PSU FAN



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### 1.3.2 Connector pin definition Module side

Pin	Pin Name	Pin	Pin Name
1	GND	2	SERIRQ
3	VDD	4	LPCPDn
5	VDD	6	LAD0
7	VDDSB	8	LAD1
9	GND	10	LFRAMEn
11	GND	12	LCLKI
13	LRESETn	14	LAD2
15	CLKRUNn	16	LAD3

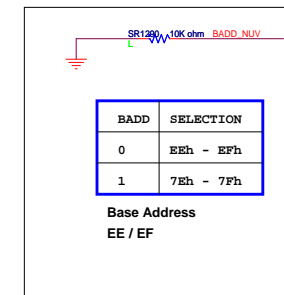
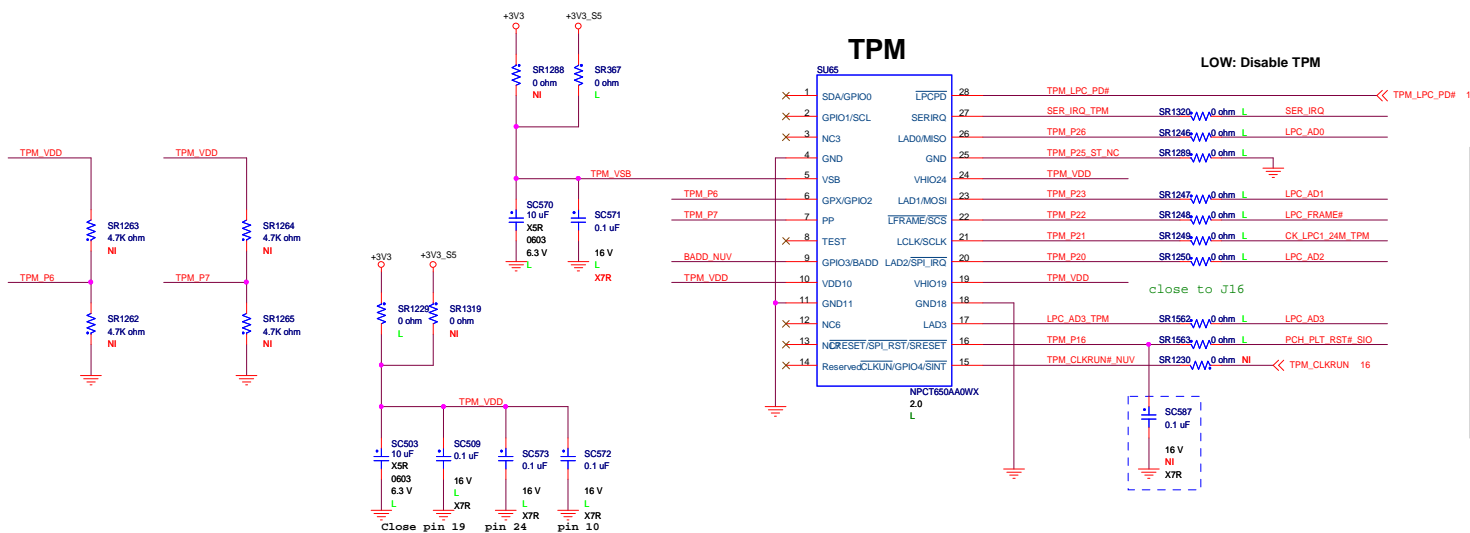


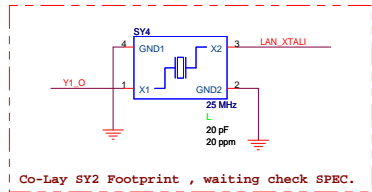
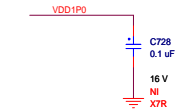
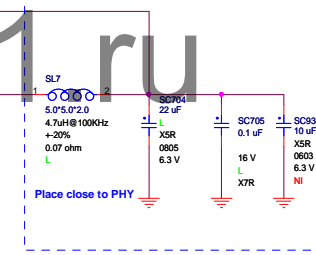
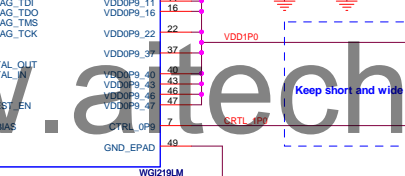
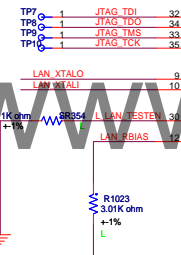
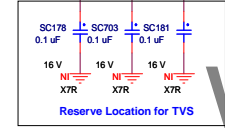
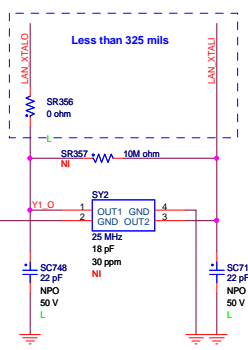
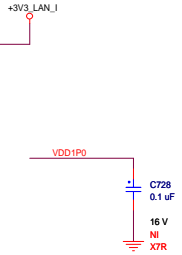
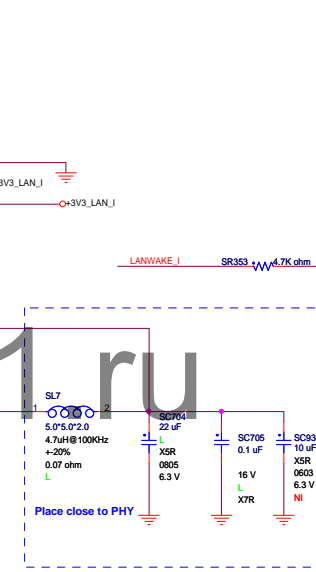
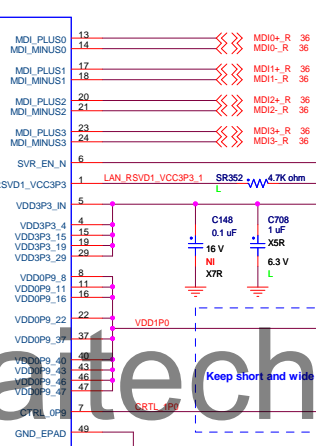
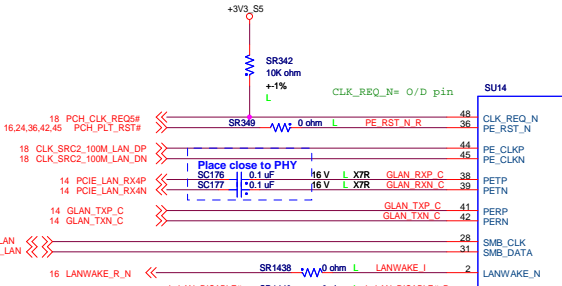
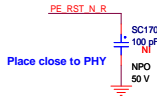
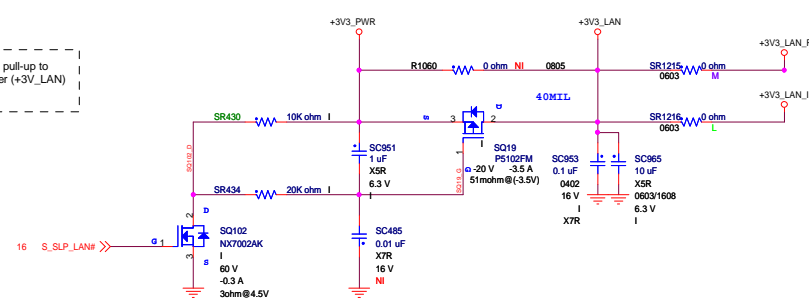
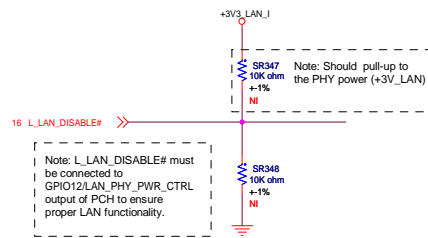
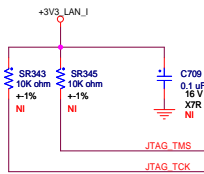
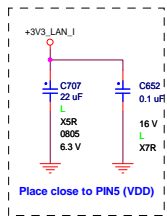
此排为双数 Pin 脚,即从左到右依次为 2,4,6,8,...14,16Pin

第2 Pin

第1 Pin

此排为单数 Pin 脚,即从左到右依次为 1,3,5,7,...13,15Pin





P5102FM Rds(on)=48mohm typ 61mohm max  
NTR4101PT1G  
Rds(on)=90mohm Typ~ 120mohm Max

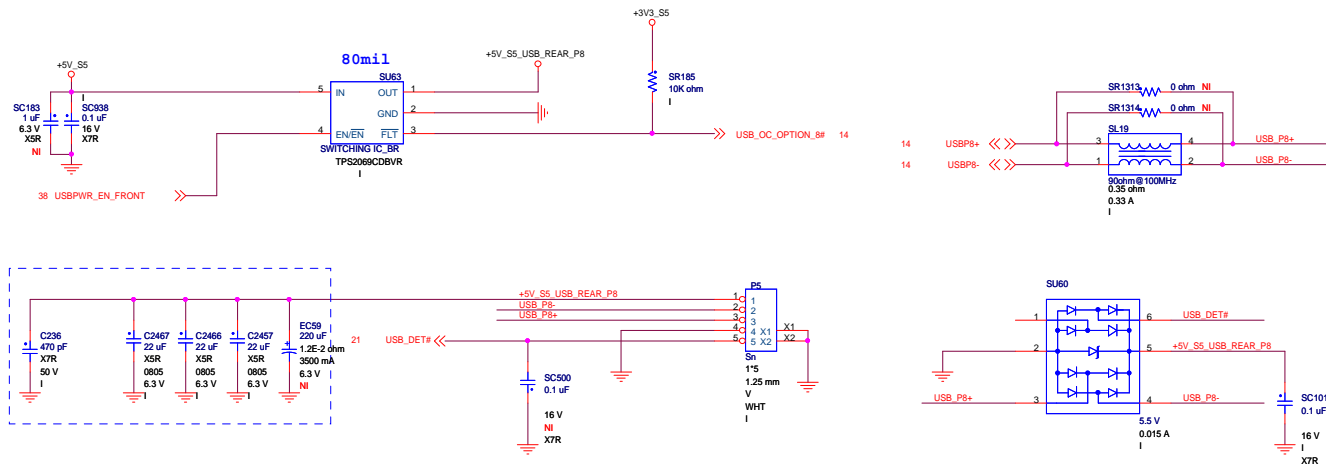
Typical LED configuration

WOL	Status	Yellow	Green	Orange
On	S3/S4/S5 Inactive	Off	Off	Off
On	S3/S4/S5 Active	Blinking	Off	Off
Off	S3/S4/S5	Off	Off	Off
On	10Mb Inactive	Off	Off	Off
On	10Mb Active	Blinking	Off	Off
On	100Mb Inactive	Off	On	Off
On	10Mb Active	Blinking	On	Off
On	1Gb Inactive	Off	Off	On
On	1Gb Active	Blinking	Off	On

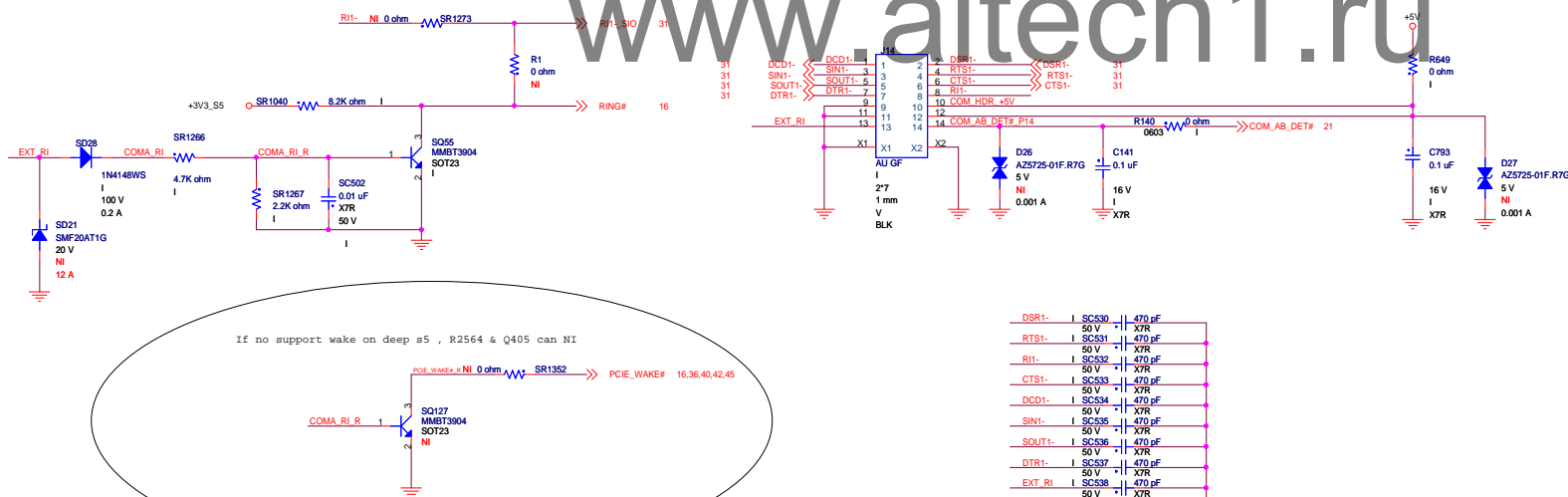




## Option USB2



## COM PORT HDR



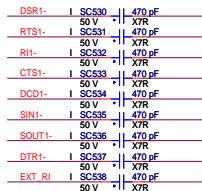
If no support wake on deep s5 , R2564 & Q405 can NI

PCIE\_WAKE# & NI 0 ohm SR1352 PCIE\_WAKE# 16,36,40,42,45

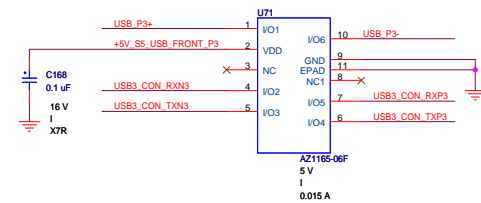
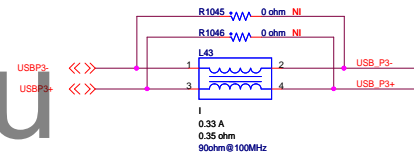
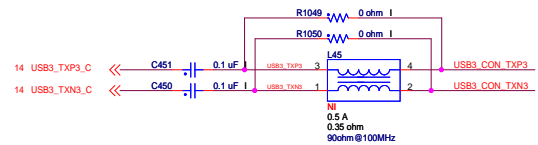
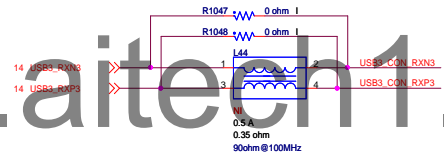
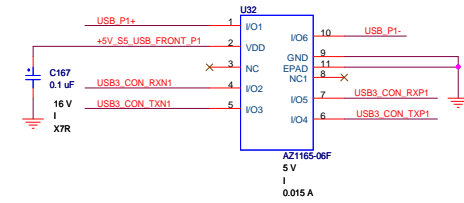
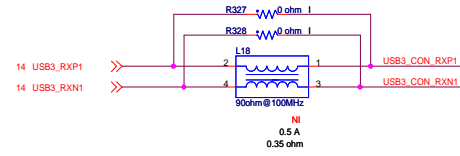
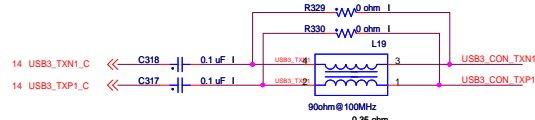
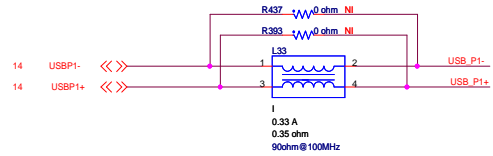
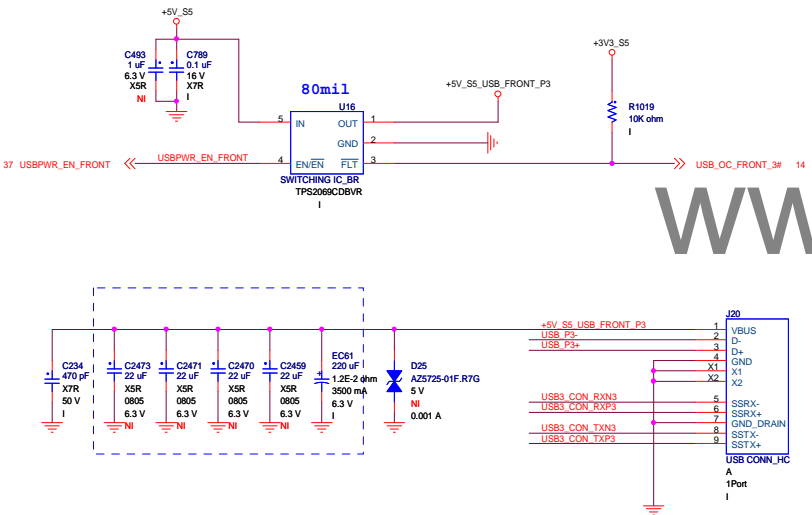
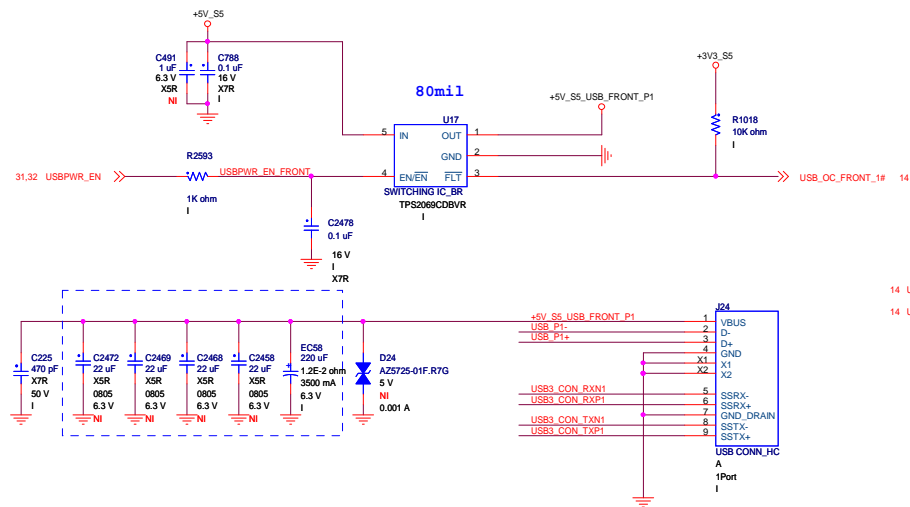
COMA\_RL\_R 1

SQ127 MMBT3904 SOT23

NI



# Front Side USBx2



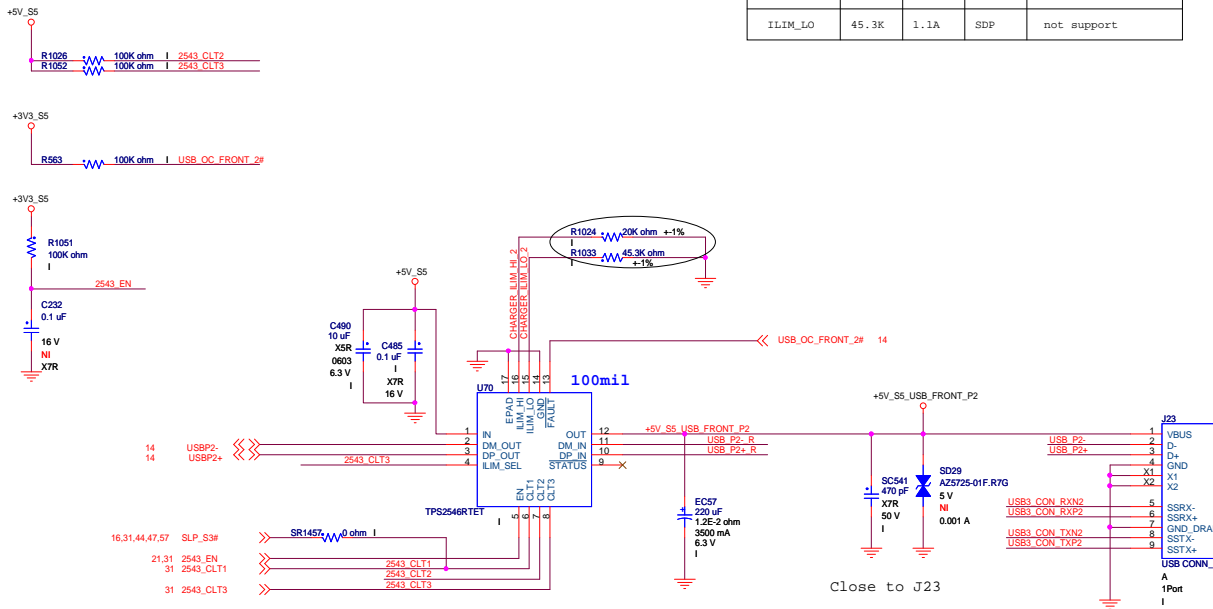
www.aitech1.ru

ILIM_HI	20K	2.5A	DCP	S3/S4/S5
ILIM_LO	45.3K	1.1A	CDP	S0
			SDP	not support

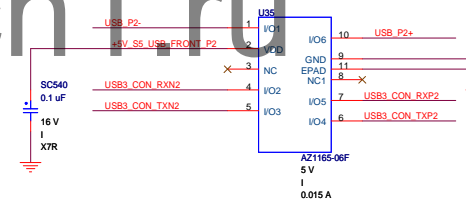
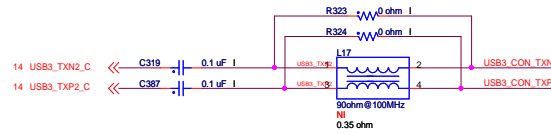
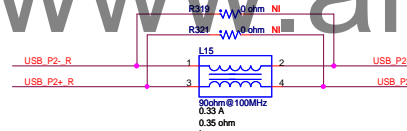
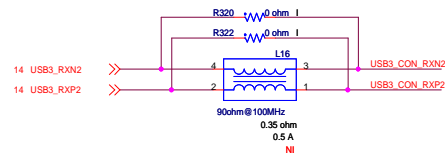
## FRONT USB3.0 Charger x 1

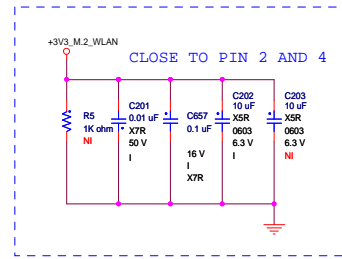
CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
0	0	0	0	Discharge	NA	off
0	0	0	1	Discharge	NA	off
0	0	1	0	DCP / auto	ILIM_HI	off
0	0	1	1	DCP / auto	ILIM_HI & I <sub>OS_PW</sub> & ILIM_HI <sup>(1)</sup>	DCP load present <sup>(2)</sup>
0	1	0	0	SDP	ILIM_LO	off
0	1	0	1	SDP	ILIM_HI	off
0	1	1	0	DCP / auto	ILIM_HI	off
0	1	1	1	DCP / auto	ILIM_HI	DCP load present <sup>(3)</sup>
1	0	0	0	DCP / Shorted	ILIM_LO	off
1	0	0	1	DCP / Shorted	ILIM_HI	off
1	0	1	0	DCP / Divider1	ILIM_LO	off
1	0	1	1	DCP / Divider1	ILIM_HI	off
1	1	0	0	SDP	ILIM_LO	off
1	1	0	1	SDP	ILIM_HI	off
1	1	1	0	SDP <sup>(4)</sup>	ILIM_LO	off
1	1	1	1	SDP <sup>(4)</sup>	ILIM_HI	CDP load present <sup>(5)</sup>

2543_CLT3	H	H	L	L
SLP_S4#	H	L	H	L
2543_EN	H	H	H	L



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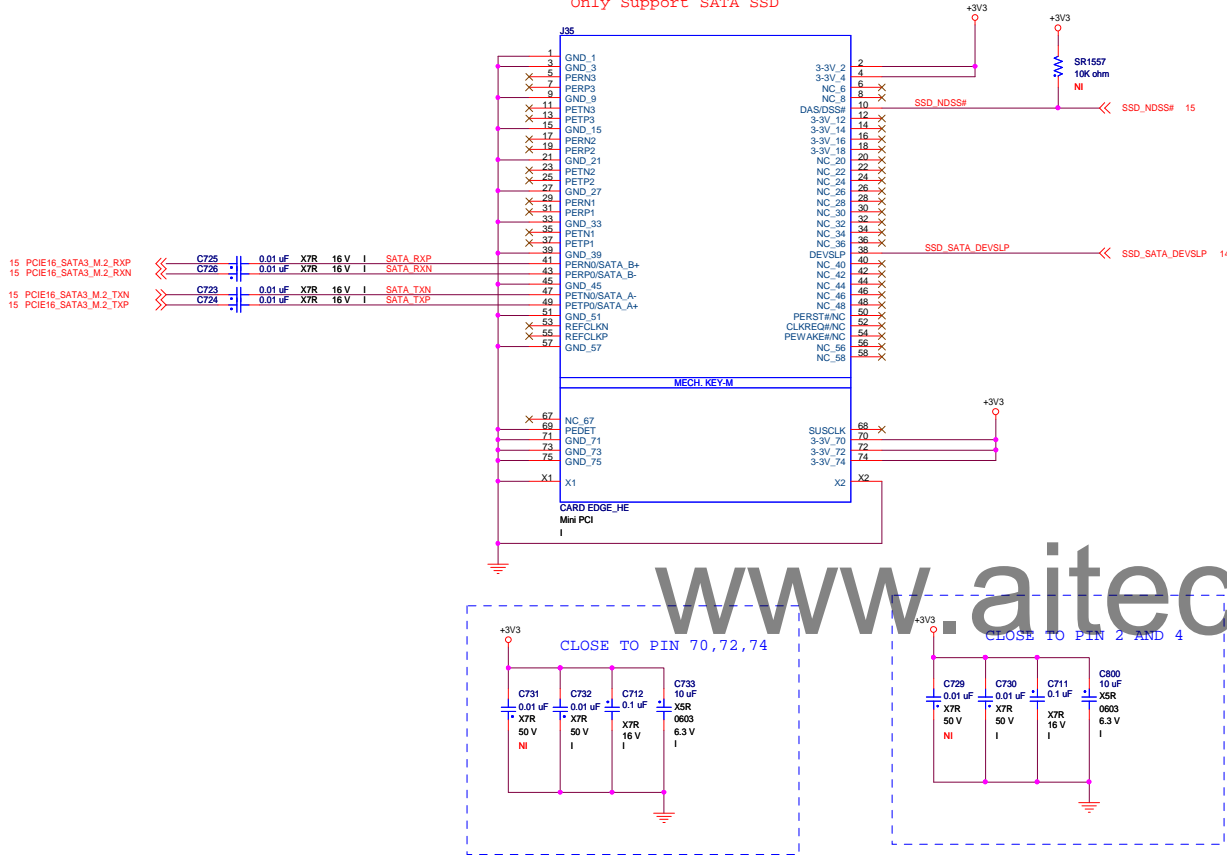




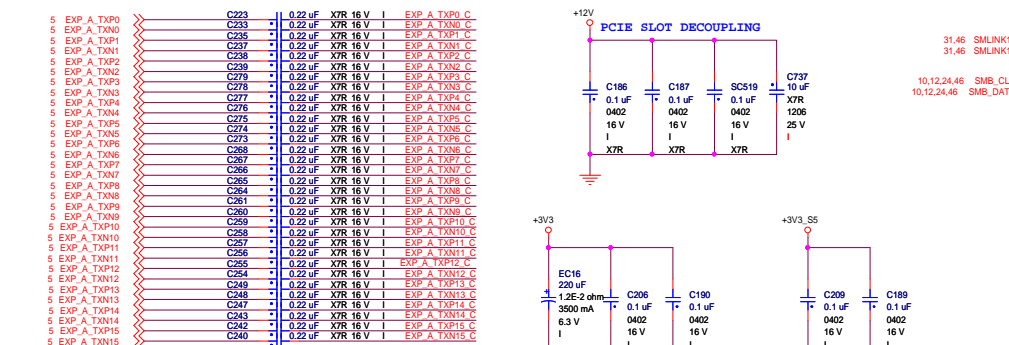
P5102FM Rds(on)=48mohm typ 61mohm max  
NTR4101PT1G  
Rds(on)=90mohm Typ~ 120mohm Max

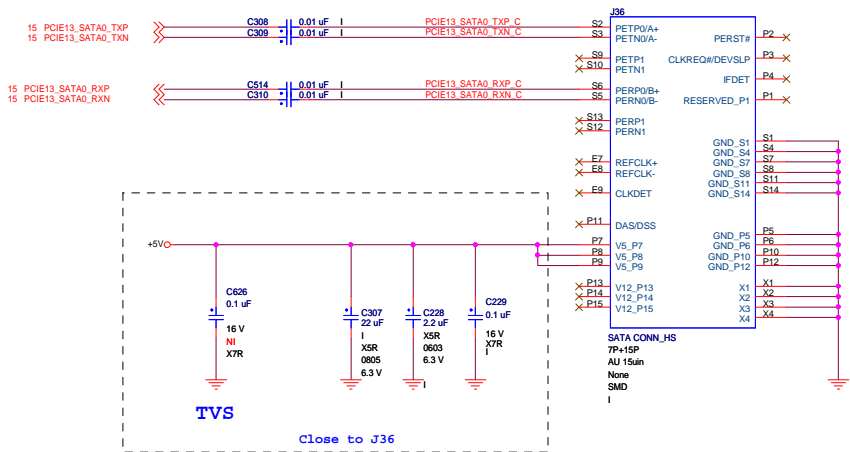
# SSD Card M.2 2242/2280 Key-M

Only Support SATA SSD



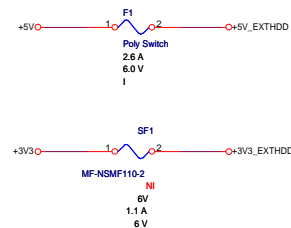
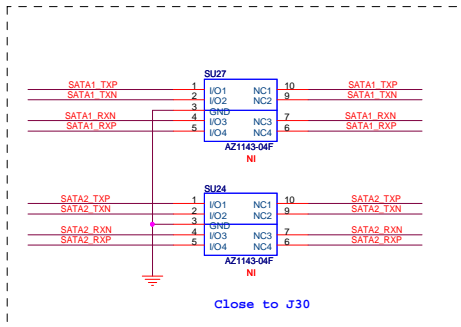
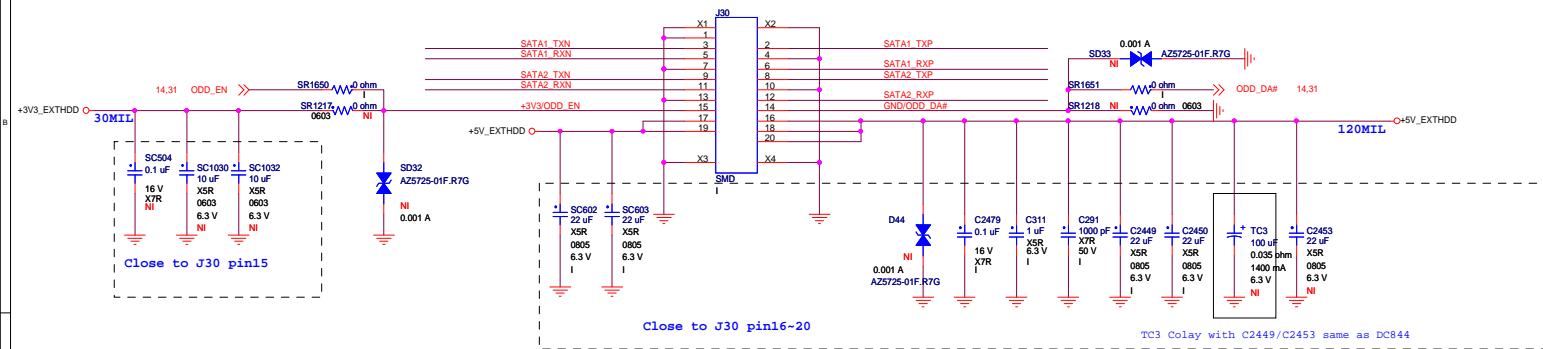
Name	Type	Description
P1	CONFIG_3	This pin is follow standard spec connect to ground.
P2	3.3V AUX	Supply pin, 3.3V
P3	GND	Ground
P4	3.3V AUX	Supply pin, 3.3V
P5	Not Available	no connect on SSD
P6	Not Available	no connect on SSD
P7	Not Available	no connect on SSD
P8	Not Available	no connect on SSD
P9	Not Available	no connect on SSD
P10	DAS#	Device Activity Signal
P11	Not Available	no connect on SSD
P12	(removed for key)	Mechanical Notch B (Removed for Key)
P13	(removed for key)	Mechanical Notch B (Removed for Key)
P14	(removed for key)	Mechanical Notch B (Removed for Key)
P15	(removed for key)	Mechanical Notch B (Removed for Key)
P16	(removed for key)	Mechanical Notch B (Removed for Key)
P17	(removed for key)	Mechanical Notch B (Removed for Key)
P18	(removed for key)	Mechanical Notch B (Removed for Key)
P19	(removed for key)	Mechanical Notch B (Removed for Key)
P20	Not Available	no connect on SSD
P21	CONFIG_0	This pin is follow standard spec connect to ground.
P22	Not Available	no connect on SSD
P23	Not Available	no connect on SSD
P24	Not Available	no connect on SSD
P25	Not Available	no connect on SSD
P26	Not Available	no connect on SSD
P27	GND	Ground
P28	Not Available	no connect on SSD
P29	Not Available	no connect on SSD
P30	Not Available	no connect on SSD
P31	Not Available	no connect on SSD
P32	Not Available	no connect on SSD
P33	GND	Ground
P34	Not Available	no connect on SSD
P35	Not Available	no connect on SSD
P36	Not Available	no connect on SSD
P37	Not Available	no connect on SSD
P38	Device Sleep Signal	If system didn't support DEVSLP, set Device Sleep Signal high and keep (from power on), device will ignore. If system support DEVSLP, set Device Sleep Signal low (from power on) device, device will support DEVSLP function as below: Device Sleep Signal H: SSD enter sleep model. Device Sleep Signal L: SSD exit sleep model.
P39	GND	Ground
P40	Not Available	no connect on SSD
P41	SATA-B-/PETn0	Host receiver differential signal pair
P42	Not Available	no connect on SSD
P43	SATA-B-/PETp0	Host receiver differential signal pair
P44	Not Available	no connect on SSD
P45	GND	Ground
P46	Not Available	no connect on SSD
P47	SATA-A-/PETn0	Host transmitter differential signal pair
P48	Not Available	no connect on SSD
P49	SATA-A-/PETp0	Host transmitter differential signal pair
P50	Not Available	no connect on SSD
P51	GND	Ground
P52	Not Available	no connect on SSD
P53	Not Available	no connect on SSD
P54	Not Available	no connect on SSD
P55	Not Available	no connect on SSD
P56	MFG1	Manufacturing pin. Use determined by vendor. Must be a no-connect on the host board.
P57	GND	Ground
P58	MFG2	Manufacturing pin. User determined by vendor. Must be a no-connect on a host board.
P59	(removed for key)	Mechanical Notch M (Removed for Key)
P60	(removed for key)	Mechanical Notch M (Removed for Key)
P61	(removed for key)	Mechanical Notch M (Removed for Key)
P62	(removed for key)	Mechanical Notch M (Removed for Key)
P63	(removed for key)	Mechanical Notch M (Removed for Key)
P64	(removed for key)	Mechanical Notch M (Removed for Key)
P65	(removed for key)	Mechanical Notch M (Removed for Key)
P66	(removed for key)	Mechanical Notch M (Removed for Key)
P67	Not Available	no connect on SSD
P68	SUSCLK	no connect on SSD
P69	CONFIG_1	This pin is follow standard spec connect to ground.
P70	3.3V AUX	Supply pin, 3.3V
P71	GND	Ground
P72	3.3V AUX	Supply pin, 3.3V
P73	GND	Ground
P74	3.3V AUX	Supply pin
P75	CONFIG_2	This pin is follow standard spec connect to ground.

[illegible]

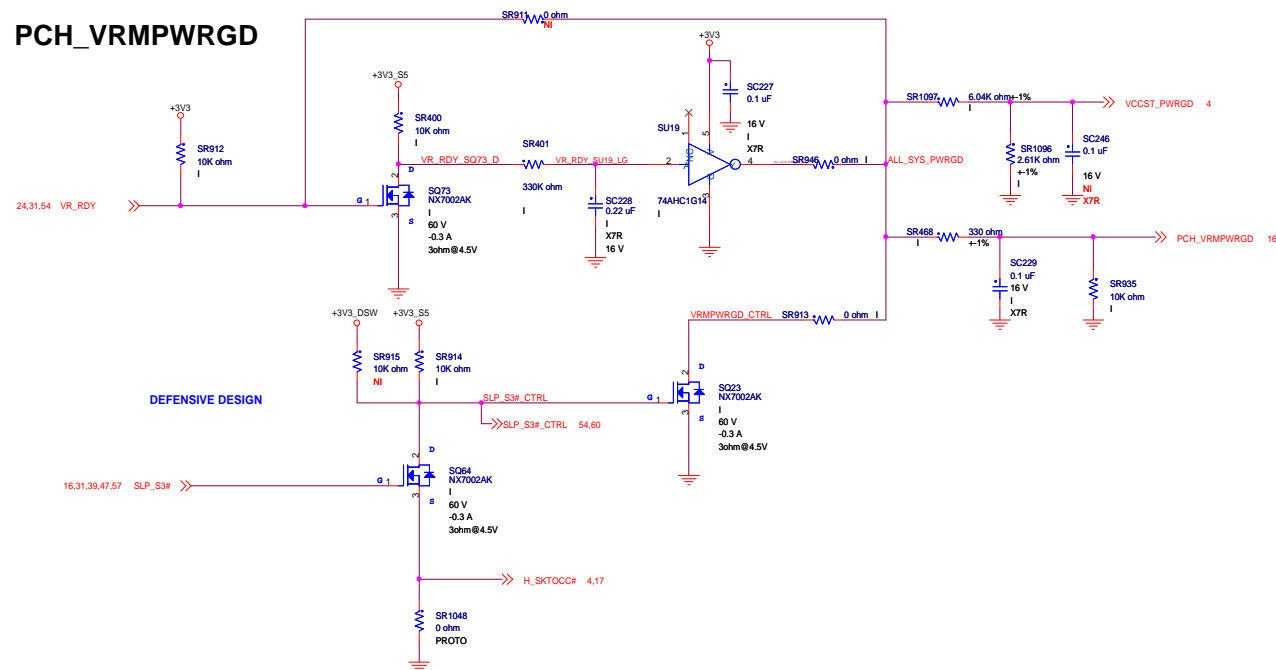


SATA FFC for 2L Box

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# PCH\_VRMPWRGD



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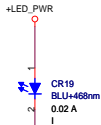


CONTROL PANEL / LED CIRCUITRY

POWER BUTTON & LED

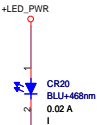
Color	Functoin
BLUE+RED	PWR
BLUE	HDD
BLUE	LAN

LAN LED



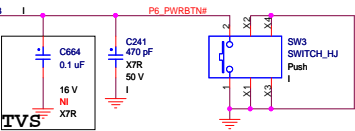
VF=2.8~3.05V  
IF=5mA  
mcd= 11.2~15

HDD LED



VF=2.8~3.05V  
IF=5mA  
mcd= 11.2~15

POWER BTN

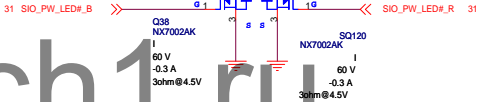


VF=3.3~3.8V  
IF=20mA  
mcd= 28~45

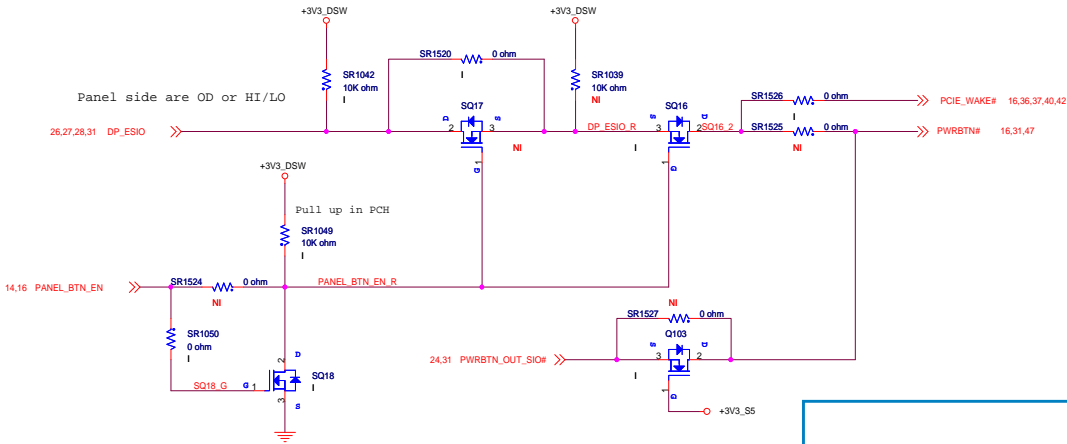
VF=2.0~2.4V  
IF=20mA  
mcd=18~45

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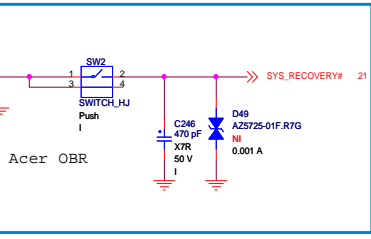
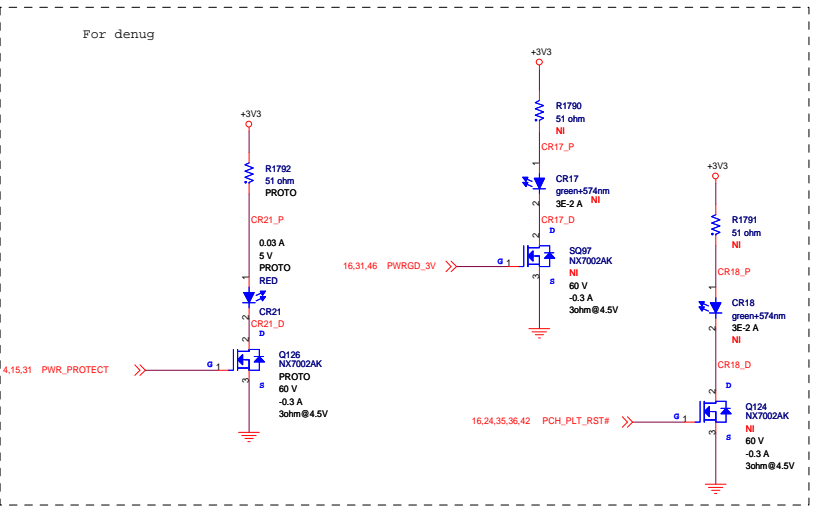
Change to SIO control power LED



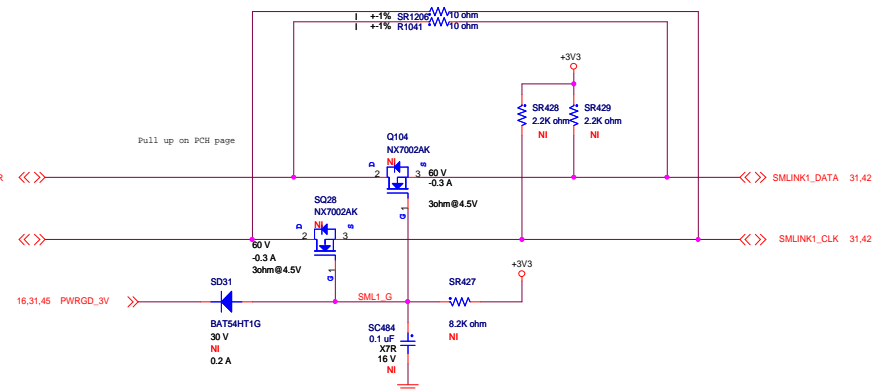
Panel side are OD or HI/LO



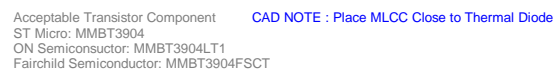
For denug



## SM Link1

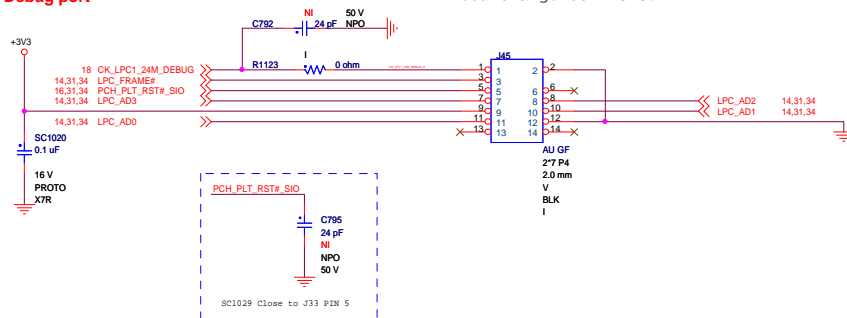
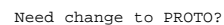


## Current Mode

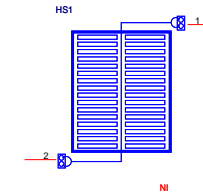
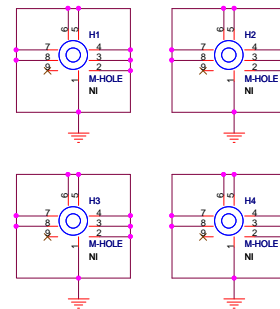
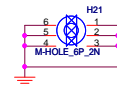


31 KDAT <<<< 2 1  
 31 KCLK <<<< 4 3  
 31 MDAT <<<< 6 5  
 31 MCLK <<<< 8 7

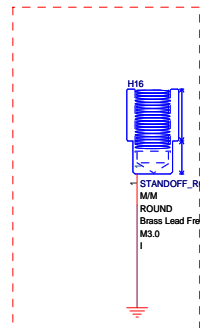
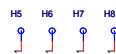
AU GF  
 2\*4  
 V  
 BLK  
 PROTO



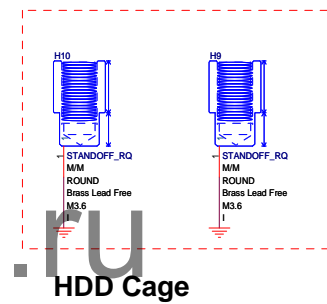
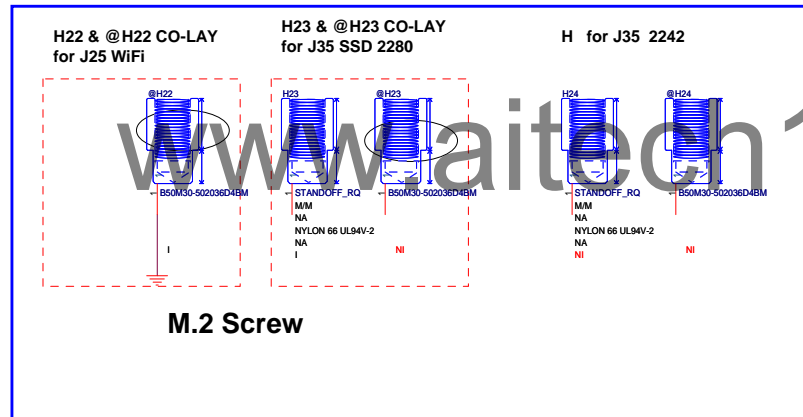
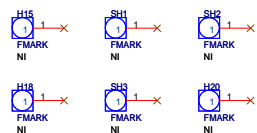
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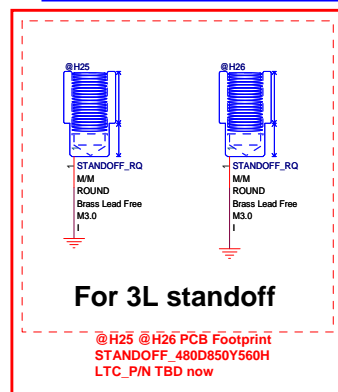
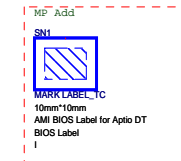
CPU HEATSINK\_HOLE



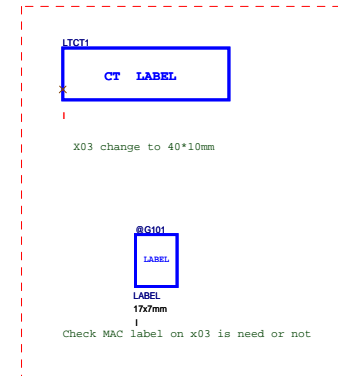
FAN DUCT




HDD Cage

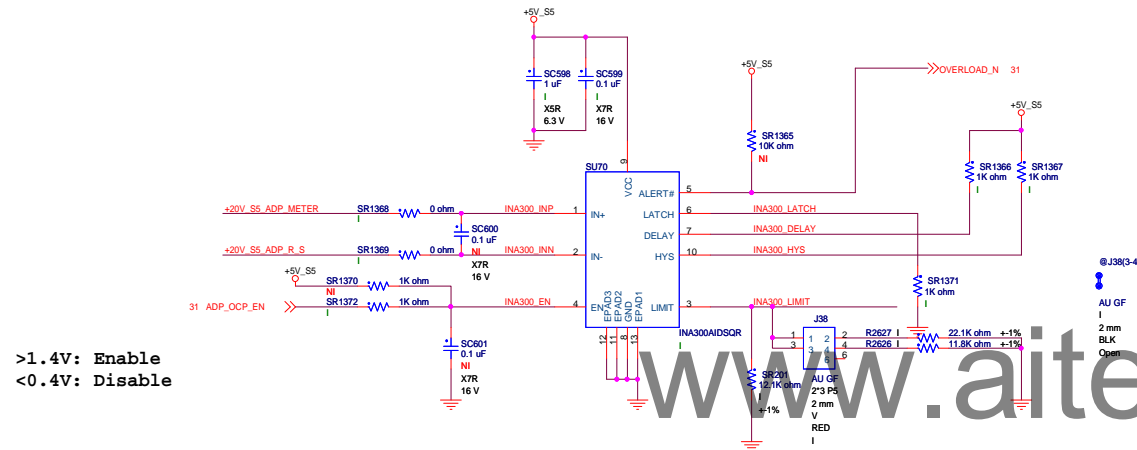
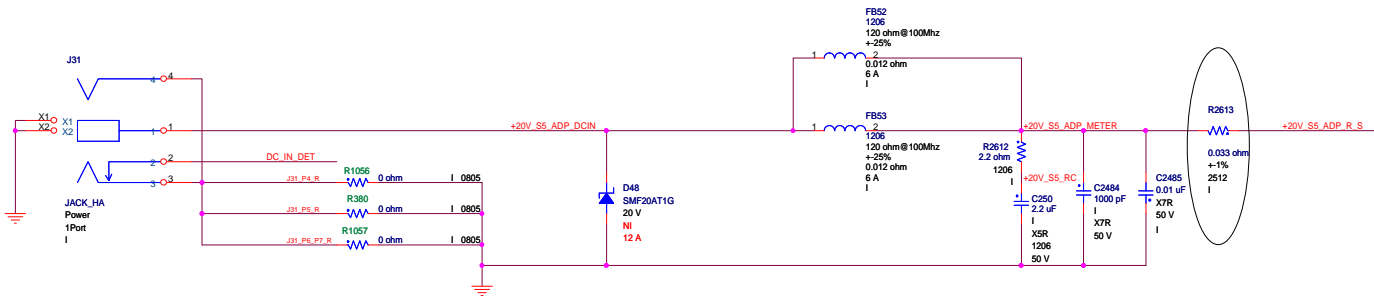


@H25 @H26 PCB Footprint  
STANDOFF 480D850Y560H  
LTC\_P/N TBD now

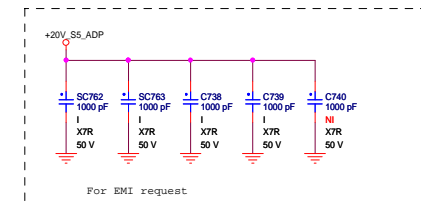


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LITE-ON TECHNOLOGY CORP.			
Title			
49. Blank			
Size	Document Number		Rev
C	MC110		X01
Date:	Wednesday, December 16, 2015	Sheet	49 of 69

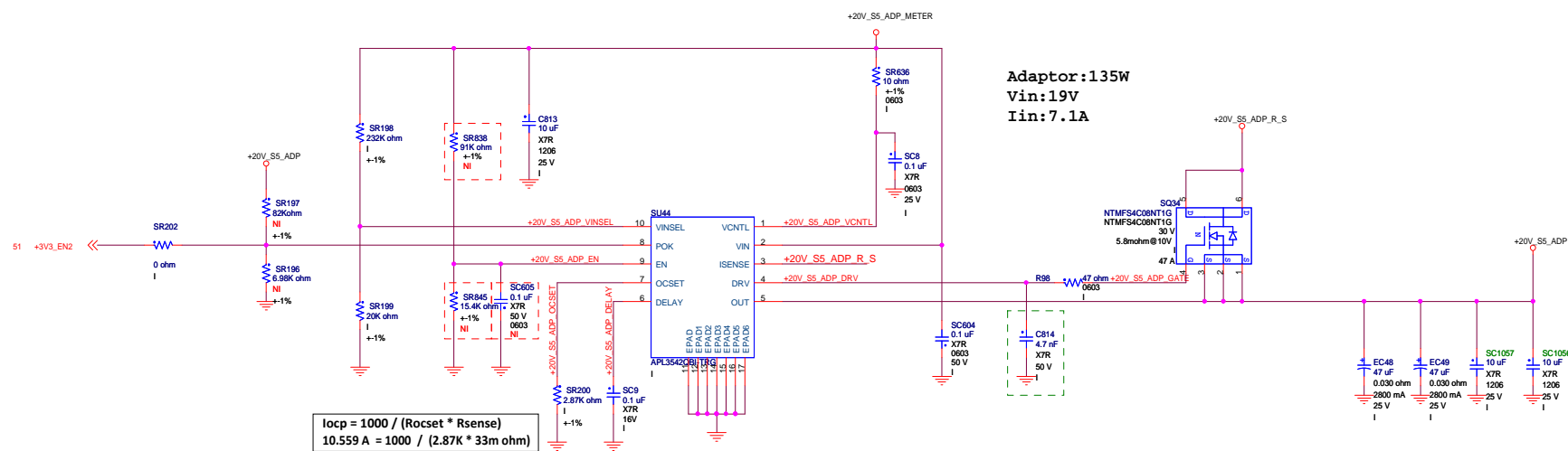


135W: 7.33A 啟動(NO JP)  
90W:5.01A 啟動(1,2)  
65W:3.62A 啟動(3,4)



>1.4V: Enable  
<0.4V: Disable

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$$I_{ocp} = 1000 / (R_{ocset} * R_{sense})$$

$$10.559 A = 1000 / (2.87K * 33m \text{ ohm})$$

Adaptor:135W  
Vin:19V  
Iin:7.1A



+5V

Please Check  
EN OFF > 2.5 V  
EN ON < 1 V

SR1044 For 8910 Install  
NTMFS4C10NT1G Solution SR104 Un-Install

SOFT-START

+5V: 5.835ms

+3V3 :3.449ms

+3V3

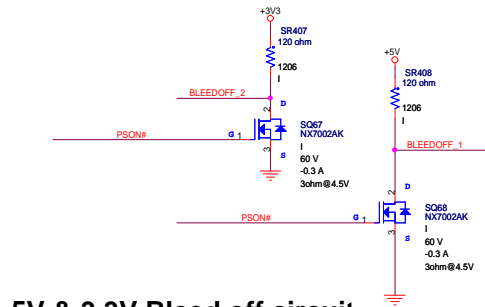
Please Check  
EN OFF > 2.5 V  
EN ON < 1 V

SR1047 For 8910 Install

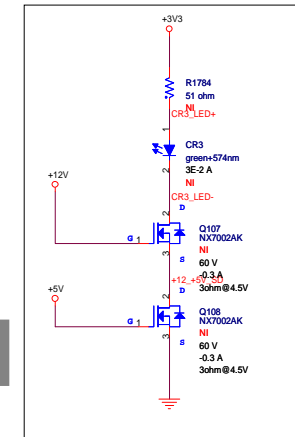
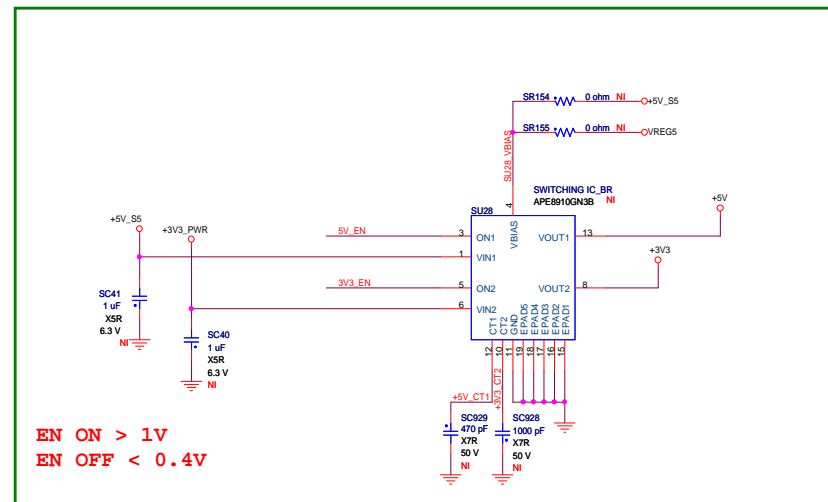
SR407 /SR408 /SQ67/ SQ68 Install For NTMFS4C10NT1G  
SR407 /SR408 /SQ67/ SQ68 Un-Install For AP8910

+3V3 @Imax 6.6A

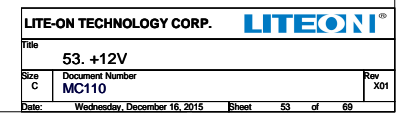
+5V @Imax 4.61A

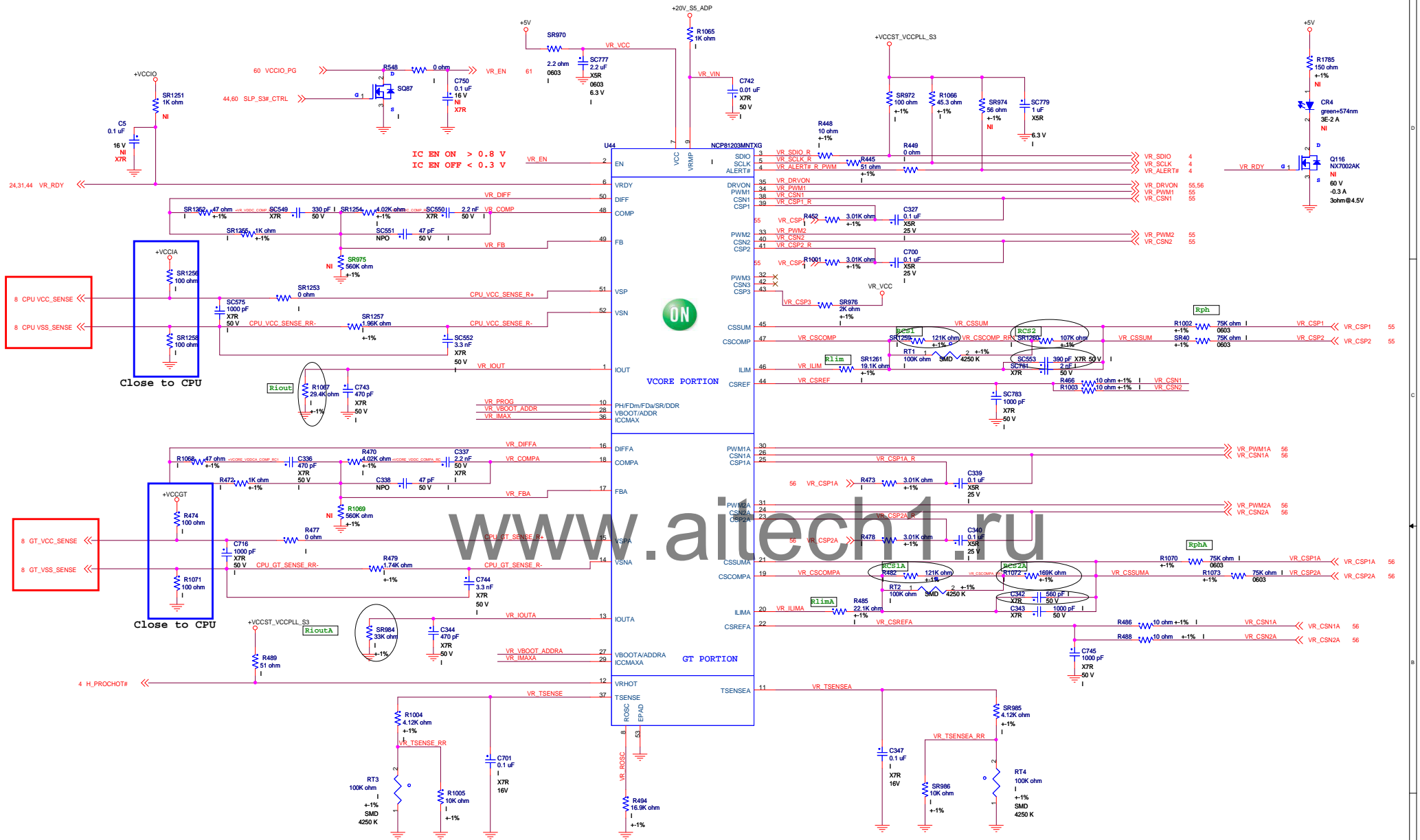


5V & 3.3V Bleed off circuit

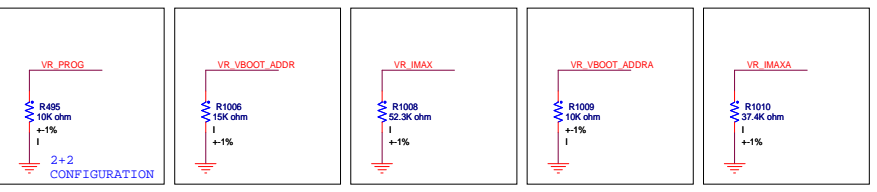






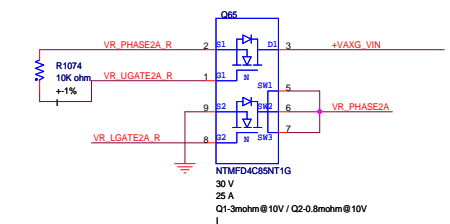


FREQ=330KHz

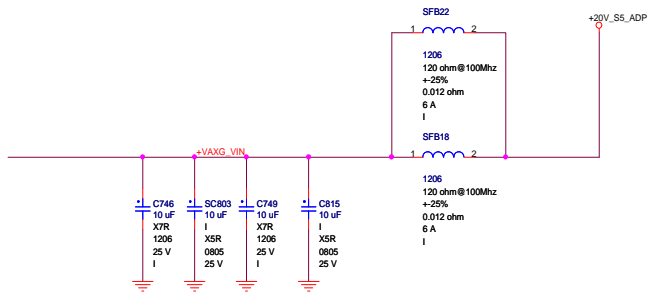
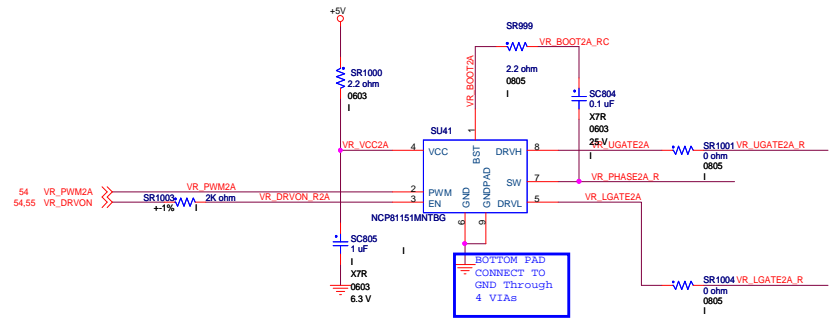


- FOR 65W CPU
- 1) R497 (52.3K) = 61.9K ..... I<sub>max</sub>
  - 2) R465 (24.9K) = 29.4K ..... OCP
  - 3) R467 (32.4K) = 35.7K ..... I<sub>out</sub>
  - 4) R499 (37.4K) = 40.2K ..... I<sub>maxA</sub>
  - 5) R485 (18.2K) = 21.5K ..... OCPA
  - 6) R487 (31.6K) = 27.4K ..... I<sub>outA</sub>

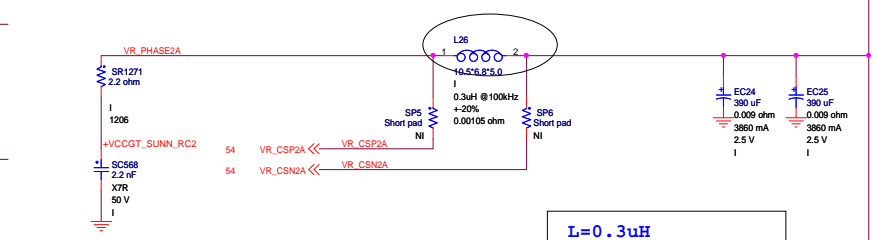




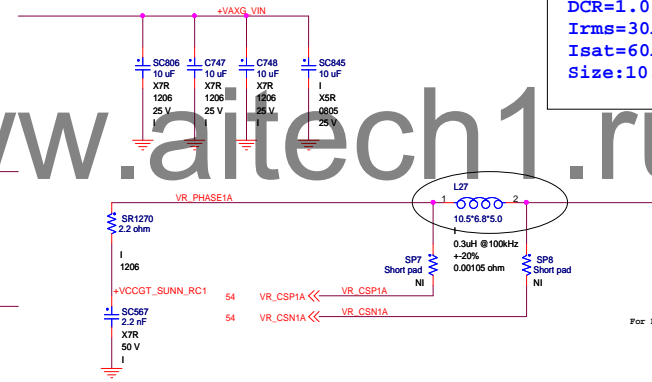
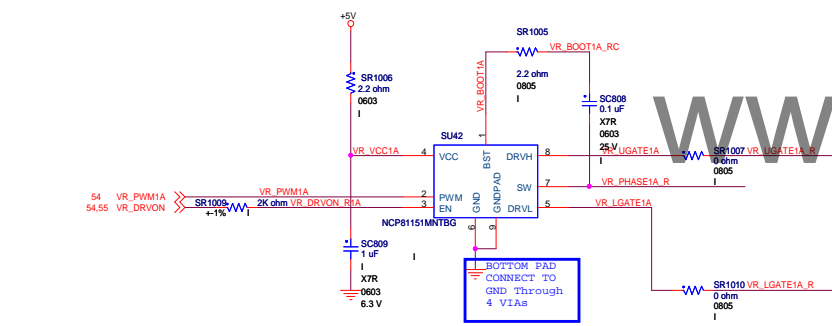
## VCCGT



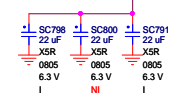
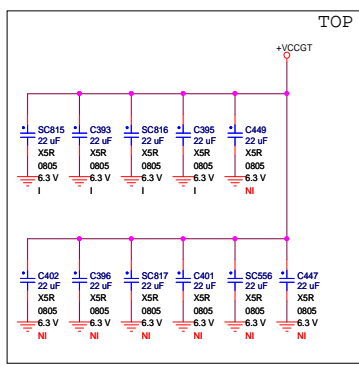
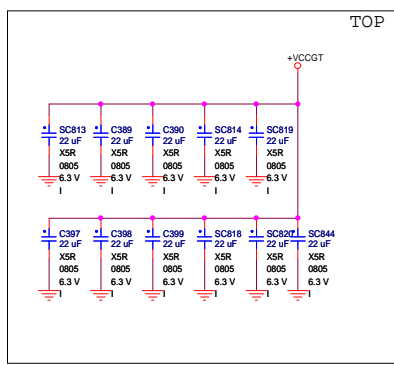
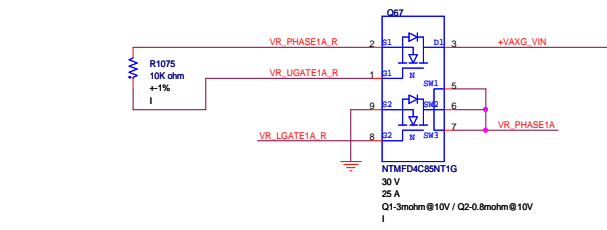
**+VCCGT**  
 Vin: +20V\_S5\_ADP  
 Vout: +VCCGT  
 Imax: 48A  
 OCP: 58.6A  
 DC LOAD LINE=3.1m  
 FSW: 330kHz



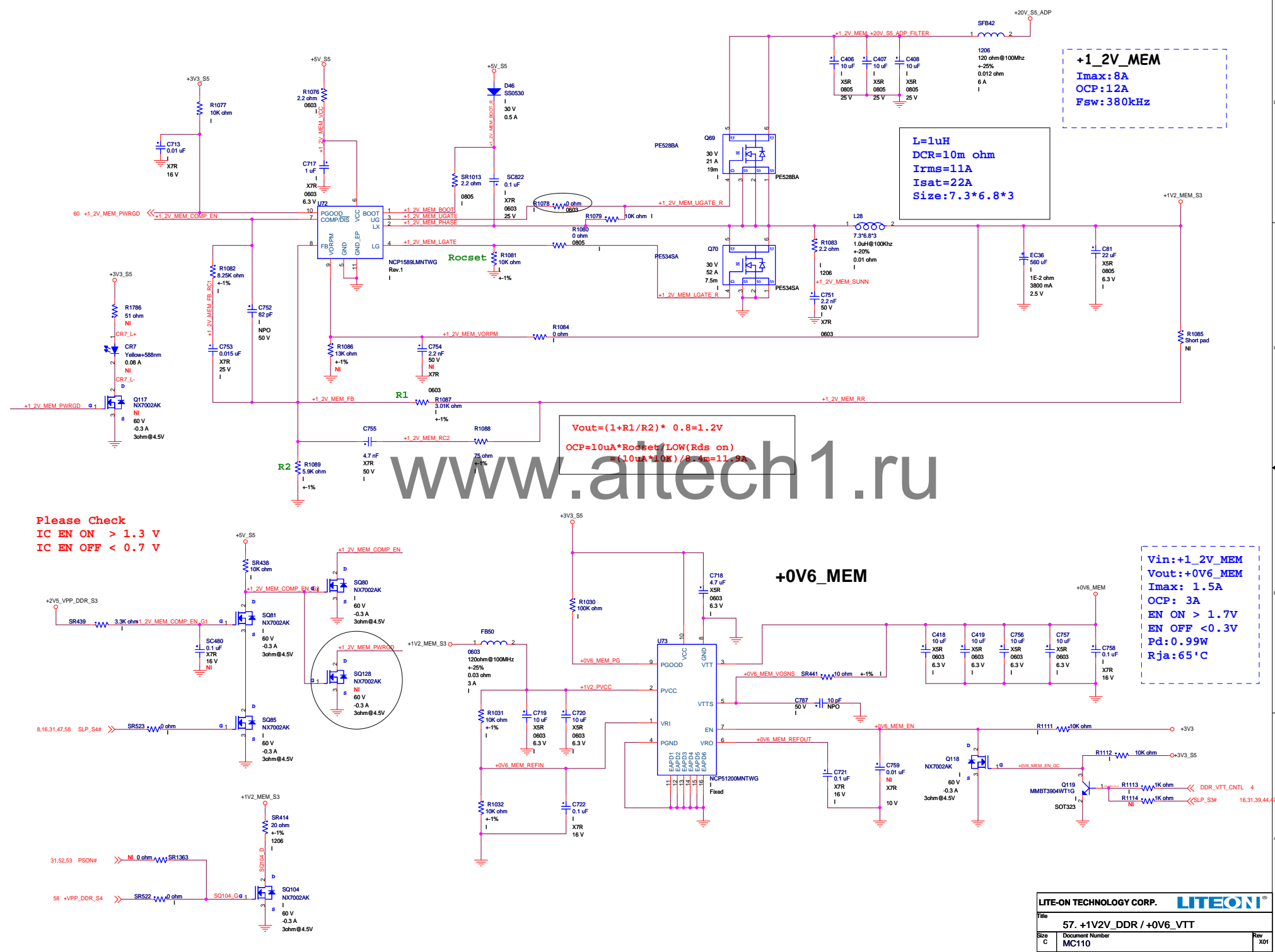
L=0.3uH  
 DCR=1.05m ohm  
 Irms=30A  
 Isat=60A  
 Size:10.5\*6.8\*5.0



For BOTTOM



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Please Check  
IC EN ON > 1.3 V  
IC EN OFF < 0.7 V

$$V_{out} = (1 + R1/R2) * 0.8 = 1.2V$$
$$OCP = 10\mu A * R_{ocset} / LOW(R_{ds\ on})$$
$$= (10\mu A * 10K) / 8.4m = 11.9A$$

## +2V5\_VPP\_DDR\_S3

### +2V5\_VPP\_DDR\_S3

Temp. Max. DC: 0.69A  
 OCP: 5.1A  
 IC EN ON > 2.7V  
 IC EN OFF < 0.4V

L=6.8uH  
 DCR=42m ohm  
 Irms=4A  
 Isat=4.8A  
 Size:6\*6\*4.5

$$V_O = V_{FB} (1 + (R_1/R_2))$$

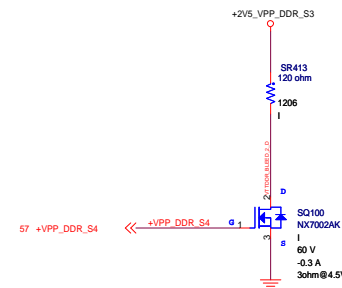
$$V_{FB} = 0.8$$

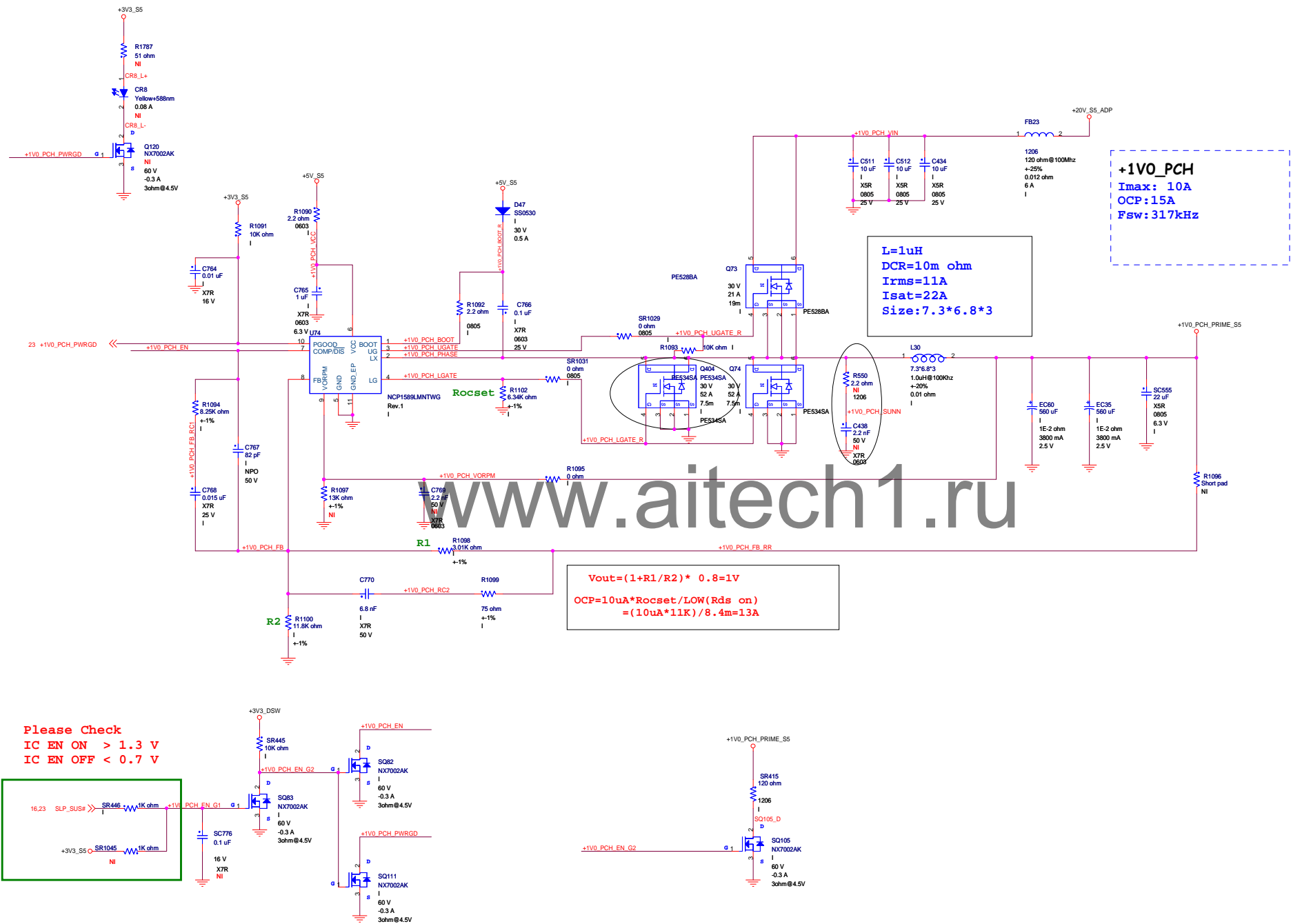
$$V_O = 5.2V$$

Please Check  
 IC EN ON > 2.7 V  
 IC EN OFF < 0.4 V

Table 1. Recommended Component Selection

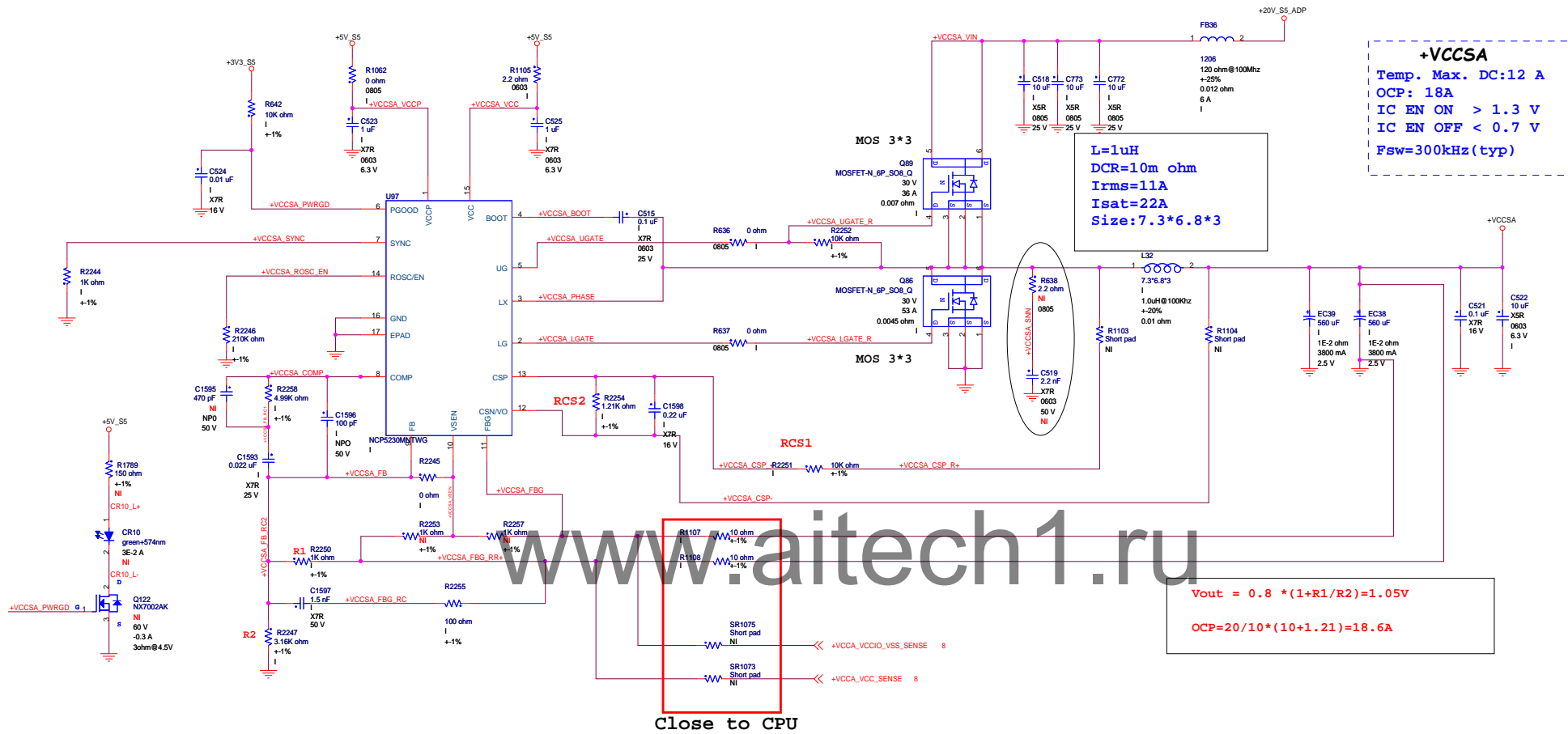
VOUT (V)	R1 (kΩ)	R2 (kΩ)	RC (kΩ)	CC (nF)	L (μH)	COUT (μF)
8	27	3	33	3.3	22	22 x 2
5	62	11.8	20	3.3	15	22 x 2
3.3	75	24	13	3.3	10	22 x 2
2.5	25.5	12	9.1	3.3	6.8	22 x 2
1.5	10.5	12	5.6	3.3	3.6	22 x 2
1.2	12	24	4.3	3.3	3.6	22 x 2
1	3	12	3.6	3.3	2	22 x 2











Please Check  
 IC EN ON > 1.3 V  
 IC EN OFF < 0.7 V

$$OCP1 = \frac{20 \text{ mV}}{\text{DCR}} \cdot \frac{\text{RCS1} + \text{RCS2}}{\text{RCS2}}$$

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Signal	Usage	When Sampled	Comment	
GSPi0_MOSI / GPP_B18	NO REBOOT 0: DISABLE (DEFAULT) 1: ENABLE	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XPDP.	
SMBALERT# / GPP_C2	TLS CONFIDENTIALITY 0: DISABLE 1: ENABLE (DEFAULT)	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.	
GSPi1_MOSI / GPP_B22	BOOT BIOS STRAP 0: SPI (DEFAULT) 1: ESPI/LPC	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h/Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap	Bit 10 Boot BIOS Destination 0 SPI 1 LPC
SML0ALERT# / GPP_C5	ESPI ENABLE STRAP 0: LPC (Default) 1: ESPI	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = LPC is selected for EC. (Default) 1 = eSPI is selected for EC.	
SML1ALERT#/ PCH#DT# / GPP_B23	EXI BOOT STALLBYPASS STRAP 0: DISABLE (DEFAULT) 1: ENABLE	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling	
GPP_H12/ SML2ALERT#	ESPI FLASH SHARING MODE STRAP 0: DISABLE (DEFAULT) 1: SLAVE ATTACHED FLASH SHARING	Rising edge of RSMRST#	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
SPI0_MISO	JTAG ODT DISABLE STRAP(DFX) 0: DISABLE 1: ENABLE(DEFAULT)	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling	
SPI0_MOSI	BOOT HALF STRAP(DFX) 0: ENABLE 1: DISABLE (PCH INT PULL-UP)(DEFAULT)	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling	
SPI0_IO2	CONSENT STRAP(DXF) 0: ENABLE 1: DISABLE	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling	
SPI0_IO3	PERSONALITY STRAP(DFX) 0: ENABLE 1: DISABLE	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling	

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- X01 to X02
- (1) Add standoff H25 & H26
  - (2) Del SR29 & R2574
  - (3) Change Realtek PCIE to port 10 from port12
  - (4) Del Standoff H22
  - (5) Change DPD\_PIN18 connect to ground
  - (6) Change SO1 to I and SR771 to NI
  - (7) Change SR1287 & R714 to 10K from 1M ohm

- X02 to X03
- (1) Del H11/H13
  - (2) Add R672 for ACPRESENT pull up to +3V3\_DSW and R655 change to NI
  - (3) Add R46 & R662 for Power on by monitor(GPD7), and R44 change to NI(GPD0) and Reserve SR1431/SR1432/R661(GPP\_B0)
  - (4) Change RJ45 SGND1/2 to system GND
  - (5) Add Audio de-pop circuit
  - (6) Change Audio jack to w/o ring type
  - (7) Change RJ45 CONN for LED define
  - (8) SC229 change to I from NI
  - (9) SR430 change to 10K & SR434 change to 20K
  - (10) SC5 change to 1uF & SR1561 change to 20K
  - (11) SR1350 change to 1k from 4.7k
  - (12) Del. colay thermal sensor Q47
  - (13) Co-lay footprint LAN 25M XTAL on SY3 &SY4
  - (14) Change R1102 to 6.34k from 12.7k ohm for 1V0\_PCH OCP setting

- X03 to X04
- (1) Change WAKE# of Realtek lan chip from LAN\_WAKE# to PCIE\_WAKE#
  - (2) Change SMBUS of Realtek Lan chip from SML0 to SMB of PCH
  - (3) Add SR65(10Kohm-I) and R661(22ohm-NI) and change SR1353 to 100K ohm from 4.7K ohm for IT6515
  - (4) Add OCP circuit in page50
  - (5) Change SR1045 to NI and Change SR446 to I
  - (6) Add R99 & Change SFB5 to NI and Change SFB7 to I for pop noise circuit
  - (7) Change ADP protection to 90W @J38(1-2) from 65W @J38(3-4)
  - (8) All of E-CAP change to POLYMER CAP

- X04 to A01
- (1) Change DC Jack to 2DC-G026-I11 from 2DC-S726-I04
  - (2) Change 2280 standoff to B50M30-502036D4BM from EML-48
  - (3) Change 2280 standoff to H70M30-19401946P1D4BM
  - (4) Change SR1524 to NI, SR1049 and SR1050 and SQ18 to I
  - (5) Change J43 to DZ11A57-H7WR-4F from DZ11A57-H4WR-4F
  - (6) Change SR1656 to 1k ohm from 10k ohm
  - (7) Reserve SR915 and SR1359
  - (8) Add R1143 for VGA pin 5 to monitor power on and R1116 /R1117 change to NI
  - (9) Reserve SR1657 & SR1659 for DASH SMBUS
  - (10) Add Reserve R1 and change SR1273 to NI
  - (11) Del J39 and Change J41 for clear CMOS
  - (12) Add SQ49 and SR772 and SR1211 for ME\_disable
  - (13) Add Q103 and SR1639 for thermal shutdown
  - (14) Change C28,C29 from 15pF to 10pF for RTC timer

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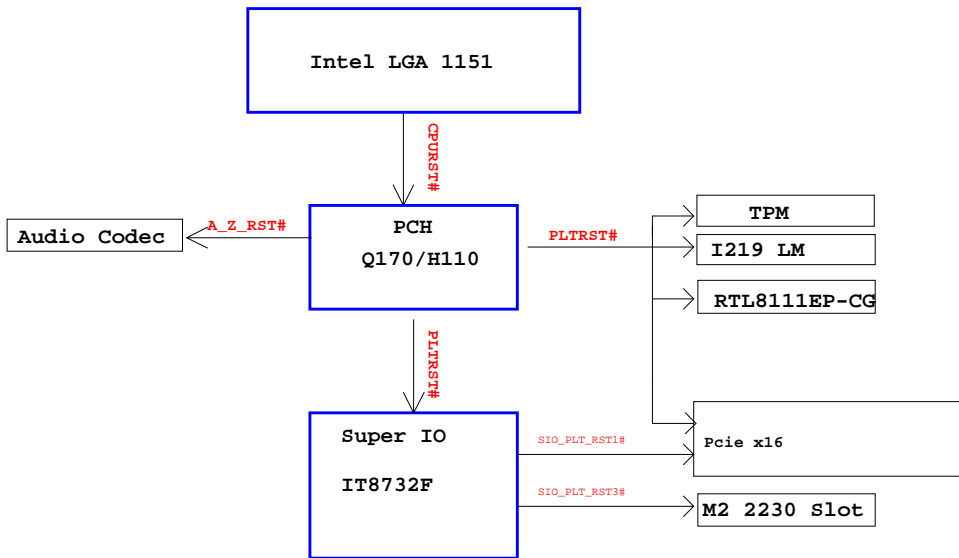
SIO IT8732F GPIO TABLE						
GPIO	Signal Name	Power Well	In/Out	ACTIVE H/L	Internal/External	MC110
GPIO_10(PIN84)	PCIRST3#/GP10	VCC3				SIO_PLT_RST3#(PU +3.3V)
GPIO_11(PIN34)	PCIRST2#/GP11	3VSB	GPO	H		SIO_PW_LED#_R (PU SB3V)
GPIO_12(PIN33)	PCIRST1#/GP12	VCC3				SIO_PLT_RST1#
GPIO_13(PIN32)	PWROK1/GP13	VCC3				PWRGD_3V(PU +3.3V)
GPIO_14(PIN31)	VCORE_EN/PC1/GP14	VCC3				SMLNK1_CLK
GPIO_15(PIN3)	PCIRST#/CIRT2/GP15/CPU_PG	3VSB	GPO	L		PWR_THROTTLE#
GPIO_16(PIN2)	SVSB_CTRL#/CRRX2/GP16	3VSB				(NO USE)
GPIO_17(PIN28)	RD#/GP17	3VSB	GPO	H		2543_CLT3_R(PU SB3V)
GPIO_20(PIN27)	CTS2#/GP20	VCC3	GPO	H		2543_EN_R(PU SB3V)
GPIO_21(PIN26)	DCD2#/GP21	VCC3	GPO	H		2543_CLT1_R(PU SB3V)
GPIO_22(PIN25)	SCK/GP22	3VSB				SIO_SCK_R
GPIO_23(PIN24)	SI/GP23	3VSB				SIO_SI
GPIO_24(PIN23)	RTS2#/GP24	3VSB	GPO	H		SIO_GP24
GPIO_25(PIN22)	DSR2#/GP25	3VSB	GPO	L		IO_SC#
GPIO_26(PIN21)	SOUT2/GP26	VCC3	GPO			OVERLOAD_N_R (PU SB3V)
GPIO_27(PIN20)	SIN2/GP27	3VSB	GPO	H		SIO_PW_LED#_B(PU SB3V)
GPIO_30(PIN19)	ATXPG/GP30	VCC3				ATXPG_SIO(PU +3.3V)
GPIO_31(PIN18)	PWMOUT / GP31	3VSB				(NO USE)
GPIO_32(PIN17)	DPWROK/GP32	3VSB				SIO_DPWROK(PU SB3V)
GPIO_33(PIN16)	SUSACK#/GP33	3VSB				(NO USE)
GPIO_34(PIN15)	SUSWAK#/GP34	3VSB				(NO USE)
GPIO_35(PIN14)	FAN_TAC4/GP35	3VSB				(NO USE)
GPIO_36(PIN13)	FAN_CTL3/GP36	3VSB				(NO USE)
GPIO_37(PIN12)	FAN_TAC3/GP37	3VSB				(NO USE)
GPIO_40(PIN79)	3VSB5V#/GP40	3VSB	GPO	H		ME_CNTL
GPIO_41(PIN78)	PWROK2/GP41	3VSB	GPO	H		PWR_PROTECT
GPIO_42(PIN76)	PSON#/GP42	3VSB				SIO_PSON#
GPIO_43(PIN75)	PANSVH#/GP43	3VSB				SIO_PB_IN (PU SB3V)
GPIO_44(PIN72)	PWRON#/GP44	3VSB				SIO_PWRBTN_OUT# (PU SB3V)
GPIO_46(PIN66)	D_RX0/SMBCLK2/GP46	3VSB	GPO			ADP_OCP_EN_SIO (PU SB3V)
GPIO_47(PIN65)	D_TX0/SMDAT2/GP47	3VSB				(NO USE)
GPIO_50(PIN48)	SO/GP50	3VSB				SIO_SO_8732
GPIO_51(PIN11)	FAN_CTL2/GP51	3VSB				(NO USE)
GPIO_52(PIN10)	FAN_TAC2/GP52	3VSB				(NO USE)
GPIO_53(PIN77)	SUSC#/GP53	3VSB				SIO_SLP_S4#
GPIO_54(PIN73)	PME#/GP54	3VSB				SIO_PME#
GPIO_55(PIN85)	RSMRST#/CRRX1/GP55	3VSB				RSMRST_SIO# (PU SB3V)
GPIO_56(PIN83)	MCLK/GP56	3VSB				MCLK (PU SB3V)
GPIO_57(PIN82)	MDAT/GP57	3VSB				MDAT (PU SB3V)
GPIO_60(PIN81)	KCLK/GP60	3VSB				KCLK
GPIO_61(PIN80)	KDAT/GP61	3VSB				KDAT
GPIO_62(PIN45)	KRST#/GP62	VCC3				KBRST#
GPIO_63(PIN6)	SLP_SUS#VLDT_EN/GP63	3VSB				(NO USE)
GPIO_70(PIN62)	KSIO/GP70	3VSB				(NO USE)
GPIO_71(PIN61)	KSII/GP71	3VSB				(NO USE)
GPIO_72(PIN60)	JP1KS00/GP72	3VSB				GP72JP1 (PU SB3V)
GPIO_73(PIN59)	KSO1/GP73	3VSB				(NO USE)
GPIO_74(PIN58)	KSO2/GP74	3VSB				(NO USE)
GPIO_75(PIN57)	KSO3/GP75	3VSB				SIO_GP75 (PU SB3V)
GPIO_76(PIN56)	KSO4/GP76	3VSB				(NO USE)
GPIO_77(PIN54)	KSO5/GP77	3VSB				(NO USE)
GPIO_85(PIN64)	IO_SC#/GP85/SMBDAT0	3VSB				(NO USE)
GPIO_86(PIN63)	GP86/SMBCLK0	3VSB				(NO USE)

over load to SIO

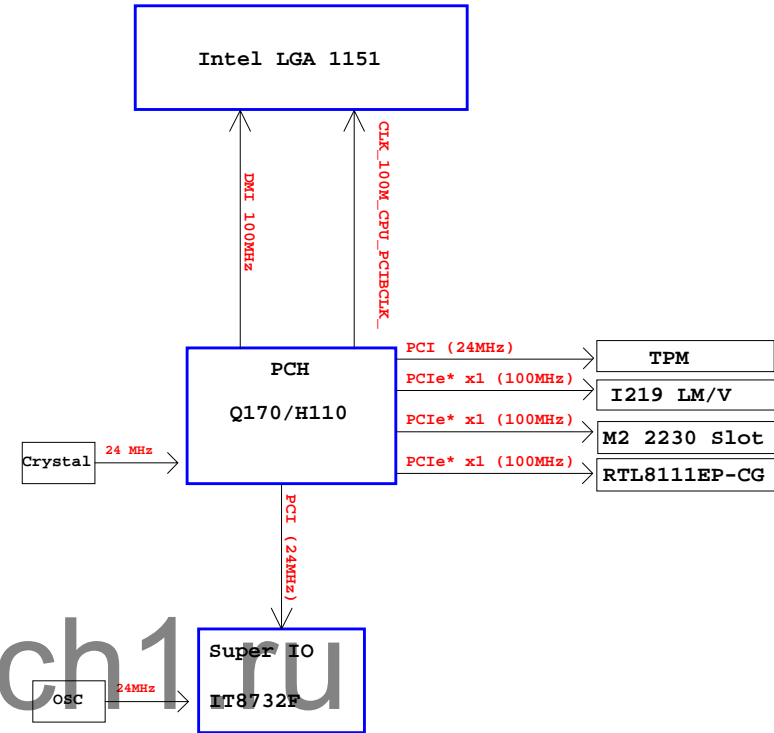
Enable current sense

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## RESET MAP

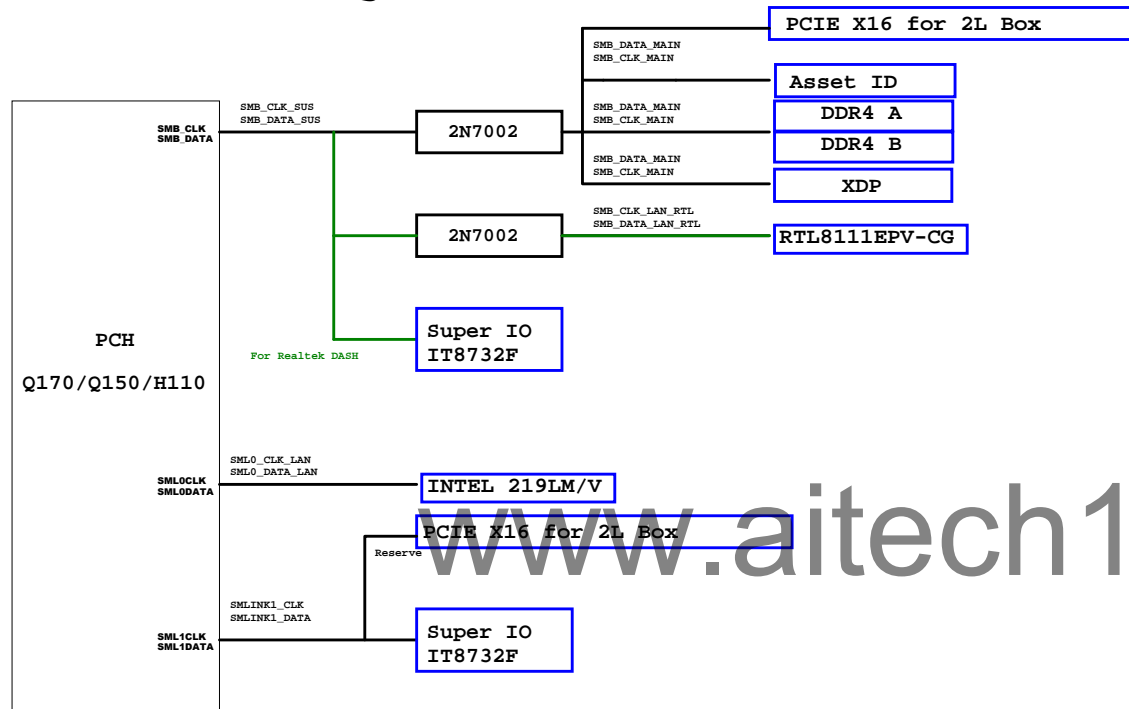


## CLOCK DIAGRAM




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## SMBUS Block Diagram





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